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Supplementary Information for

Non-associative Learning Implemented by Memristorbased Multi-terminal Synaptic Device

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Fig. S1 Schematic of device structure and measurement. (a) The fabricated device consist of an HfOx- based RRAM and a NMOS transistor. (b) The measurement schematic. Agilent B1500 and its pulse generator unite are both used.

The device used in our experiment was a three terminal (Gate, Source and Drain, represented by G, S, D respectively) device consisting of one HfO_x-Based memristor and one NMOS transistor, as shown in Fig. S1a. The memristor was integrated on the tungsten plug elicited from NMOS Drain. All the process is compatible with standard CMOS technology. Agilent B1500 with its PGU is a signal source that could implement not only direct current (DC) sweeping but also pulse stimulations with flexible programmable shape and frequency. Four channels are provided and each can output either DC or pulse stimulation signals. In our experiment four channel are used, two channels are connected to G and the substrate to import DC signals while the other two are connected to S and D to import DC or pulse signals modulated by PGU selector. The pulse series applied are with 1ms width, 10ms ~ 100ms interval. Especially, we defined all pulses used in our experiment were positive in value. And then the pulses load in the Drain is defined as positive while the pulses load in the Source are defined as negative because of its opposite direction compared to positive pulse.



Fig. S2 the DC switching characteristic of memristor-based multi-terminal device and single memristor.

The memristor cell is connected in series with the Drain terminal of MOSFET transistor, so the inside of our device can be regarded as a voltage divider (R_T+R_M). From the IV sweep of memristor-based multi-terminal device depicted above(Fig. S2a), we can clearly observed that the RESET voltage is lager than SET voltage. The difference between switching voltages is mainly ascribe to the different resistance state of memristor cell in the voltage divider system by comparing the switching characteristics between memristor-based multi-terminal device (Fig. S2a) and single memristor (Fig. S2b) (The two devices are in the same wafer and fabricated in the same process). In the SET process, the memristor cell is at a high resistance state (HRS) at the beginning, so the voltage drop across the memristor cell can easily reach its switching threshold due to its higher resistance state (LRS) at the beginning, so in order to ensure the voltage across the memristor cell can switch it, the RESET voltage must be larger ($R_{M-LRS}+R_T$ and $R_{M-LRS} < R_T$) so that the memristor cell with a low resistance state can get a voltage that reaches the switching threshold. This is why the RESET voltage is larger than SET voltage. In the same way, the amplitude of pulse stimulus applied in Source (for RESET) is larger than that applied in Drain (for SET).

Besides, from the IV characteristics of both two devices, it is clearly that the modulated effect of transistor on memristor cell conductance change. For the single memristor device, the SET is an abrupt process, while the memristor-based multi-terminal device shows a gradual resistance change process. It is mostly due to the voltage-divided effect of the transistor. In the SET process, the voltage acrocss the memristor cell of the R_T-R_M voltage divider may gradually decrease as its resistance become smaller and smaller, which is different from the SET process in single memristor. Thus the memristor-based multi-terminal device has good gradual resistance tuning property.



Fig. S3 Th (b) anergy Dispersive X-ray) analyzation and DC gradual conductance tuning characteristic. (a) The element. (b) The current modulation in response to successive DC sweeps.

We performed Energy Dispersive X-ray (EDX) to analyze the specific distribution of each element, as shown in Fig. S3a. Definitely, a clear lateral hierarchical structure can be seen from the EDX, a stack of W/TiN/Ti/HfOx/W from the top to end. Then we implemented the gradual conductance tuning characteristic of our memristor-based multi-terminal device both under DC sweeps and pulse stimuli. The gradual conductance modulated by voltage pulses has already been demonstrated in Fig. 2b, here we discuss the device conductance varying under the application of continuous DC voltage sweepings. Consecutive DC voltage sweep from 0V to 400mV loads in the Drain for SET process and voltage sweeps from 0V to 430mV loads in the Source for RESET process respectively. And the voltage at Gate is 1.5V while the Substrate was grounded. The Source and Drain was grounded alternately while the other applied stimulation signals. It can be clearly seen from Fig. S3b that the device conductance (represented by measured current) continuously increases by the presentation of consecutive positive sweeps and decrease by the following negative sweeps. These gradual conductance changing characteristics indicates that our device

can effectively show potentiation and depression plasticity as the bionic synapse, which offers advantages in the implementation of non-associative learning behaviour.



Fig. S4 Schematic illustration of the device conductance change in the RESET process (a) and SET process (b). The direction of the arrow is an example of the movement of an oxygen ions.

The conductance change mechanism of oxide-based memristor has been well studied, and it is widely accepted that the movement and distribution of oxygen ions/vacancies in the switching layer are the main reasons (Refs S1-S4). Simultaneously, the movement of oxygen ions/vacancies is determined by not only the drift process, but also the Fick's and Soret diffusion processes (Ref S5). More importantly, all of the processes are strongly affected by the local temperature, as demonstrated in the Refs. S5 and S6 that the temperature was regarded as the second-state variable in the resistant changing. The inner temperature (T_{CF}) may increase when a pulse stimulus was applied due to the Joule heating and then decay spontaneously after the pulse is gone, which provides an internal timing dependent mechanism.

In the RESET process, the P_{drift} (drift process of oxygen ions/vacancies) is strengthened because of the high electric field between the CF tip and the top electrode, as well as the high temperature caused by the large reset current. Besides, the P_{Fick} and P_{Soret} are also increase due to the increased temperature. As shown in Fig. S4a, the influences of these three process are in the same direction and lead to a decrease of device conductance. When the pulse stimulus is presented with a short interval, elevated temperature will be achieved to accelerates the movement of oxygen ions/vacancies and results in a large conductance decrease. On the contrary, when the pulse stimulus is presented with a long interval, the Joule heating caused by each pulse stimulus tends to be weakened and the temperature would be hardly increased, resulting in a slow decrease of device conductance.

However, during the SET process, the temperature of CF is lower than that during the RESET process due to the lower operation current. In this case, the P_{drift} and P_{Fick} become dominant in the movement of oxygen ions/vacancies, as depicted in Fig. 4b. When the pulse stimuli is applied, the oxygen ions will be driven into the TE. And the ions that have not been driven into TE may diffuse back (the Fick's diffusion) to recombine with the vacancies when the pulse stimulus is removed. If the next pulse stimulus arrives before the oxygen ions recombine with vacancies, elevated oxygen concentration can be achieved to form a robust CF. Thus the extent of device conductance depending on the size of CF is in turn modulated by the interval time between the pulse stimuli. That is to say, when the pulse stimuli is presented with a short interval, the Fick's diffusion process can be effectively restrained and the drift process become more dominant, thus more concentration oxygen vacancies will be gathered to form a robust CF, as well as an apparent increase of device conductance. This is the main reason for the frequency-dependent performance of our devices.

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