

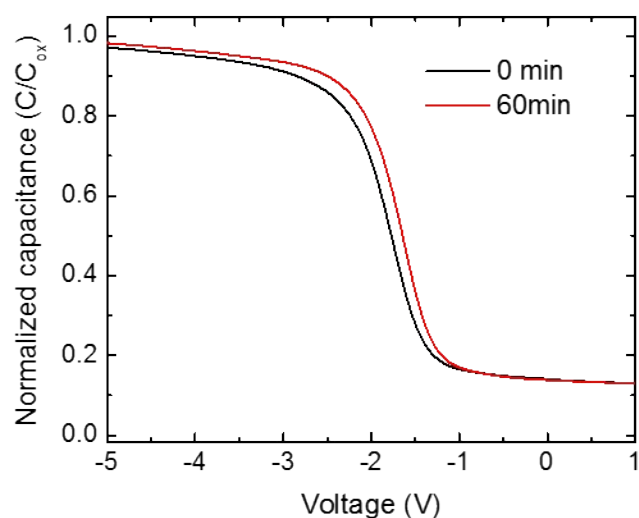
## Supporting Information

### Transfer-free Multi-layer Graphene as a Diffusion Barrier

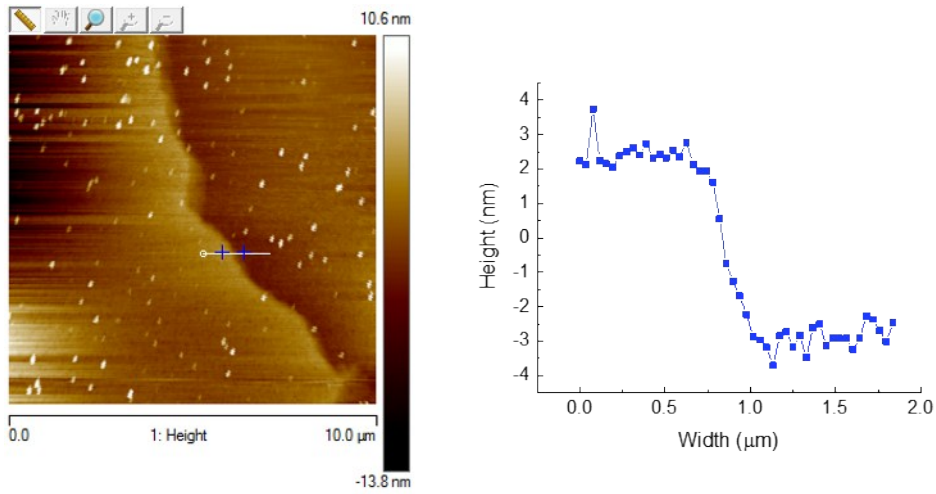
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<sup>a</sup> School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, 1205 W State Street, West Lafayette, IN 47907, USA. E-mail: zhchen@purdue.edu

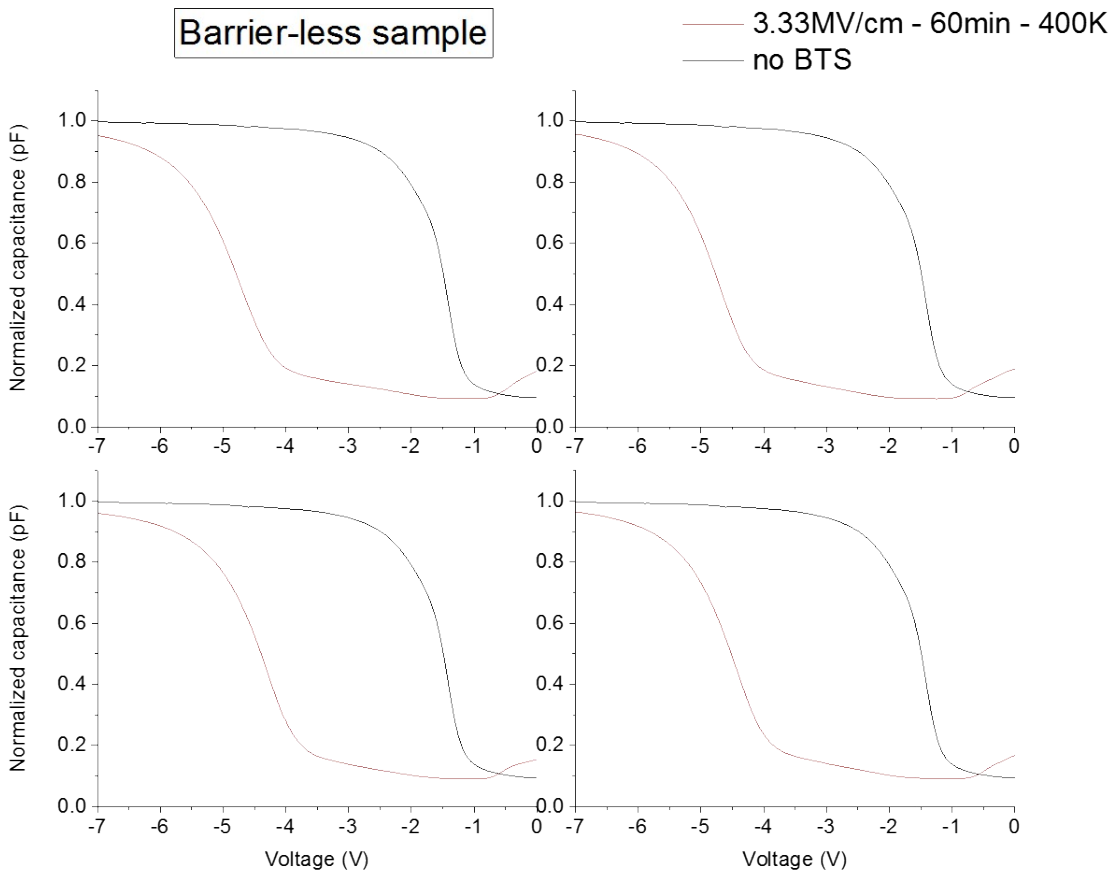
<sup>b</sup> Intel Corporation, 2501 NW 229th Avenue Hillsboro, OR 97124, USA.



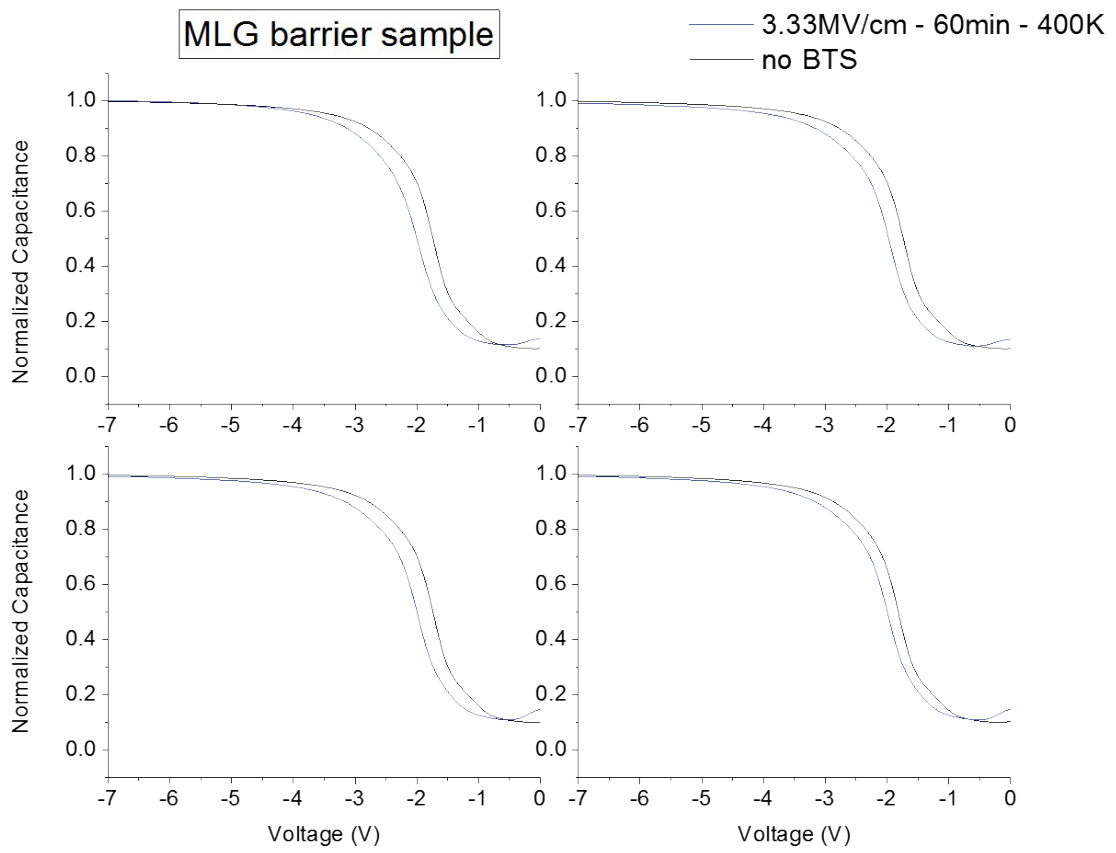
**Figure S1.** Normalized capacitance as function of DC voltage (@ 100kHz AC excitation) for the barrier-less sample without pre-oxidation of Cu electrode. We did not observe flatband voltage shift in the negative direction after 60min BTS due to lack of Cu ion generation under vacuum.



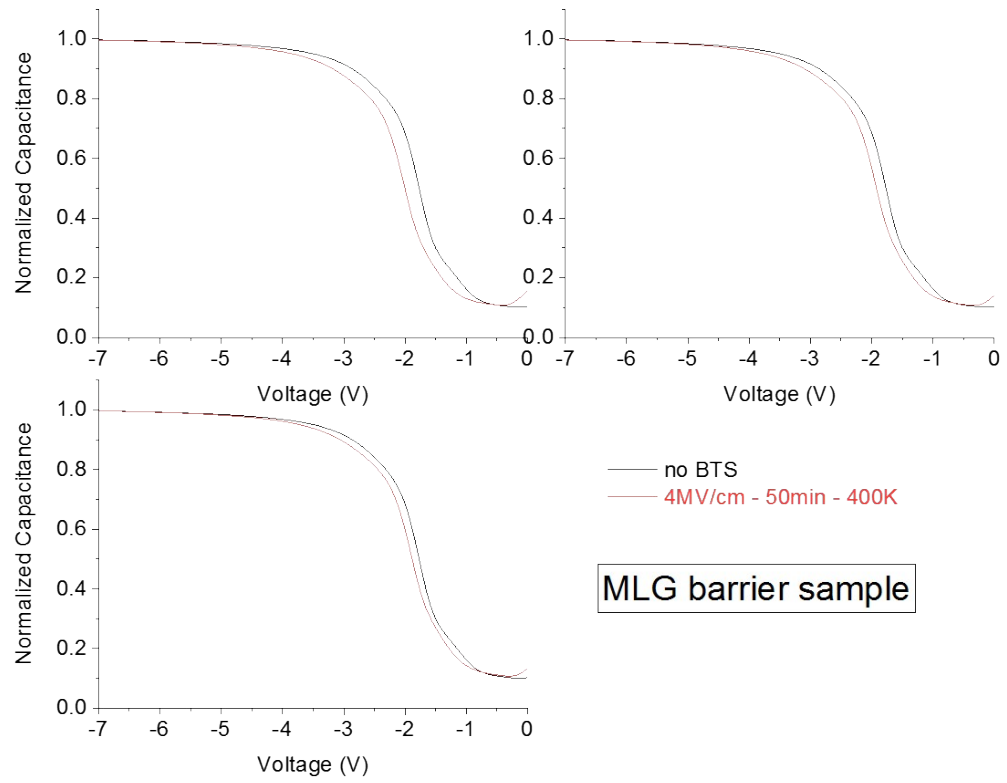
**Figure S2.** Atomic force microscopy scan and height data for evaporated Ta on SiO<sub>2</sub>. Average Ta thickness was 5nm and the coverage was uniform.



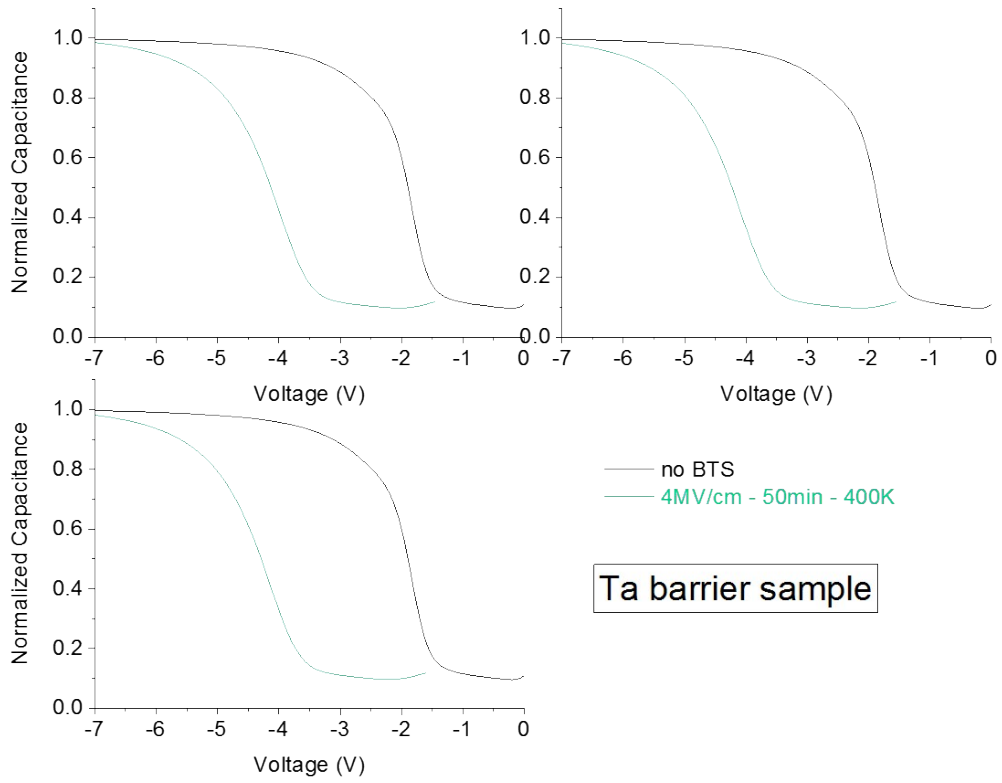
**Figure S3.** Normalized capacitance as function of DC voltage for the barrier-less sample measured on different dot capacitors. All capacitors have flatband voltage shift matched to within  $\pm 0.2$  V.



**Figure S4.** Normalized capacitance as function of DC voltage for the MLG barrier sample measured on different dot capacitors. All capacitors have flatband voltage shift matched to within  $\pm 0.08$  V.



**Figure S5.** Normalized capacitance as function of DC voltage for the MLG barrier sample measured on different dot capacitors. All capacitors have flatband voltage shift matched to within  $\pm 0.05$  V.



**Figure S6.** Normalized capacitance as function of DC voltage for the Ta barrier sample measured on different dot capacitors. All capacitors have flatband voltage shift matched to within  $\pm 0.2$  V.