# Supporting Information

## High-Efficiency, Hybrid Si / $C_{60}$ Heterojunction Solar Cells

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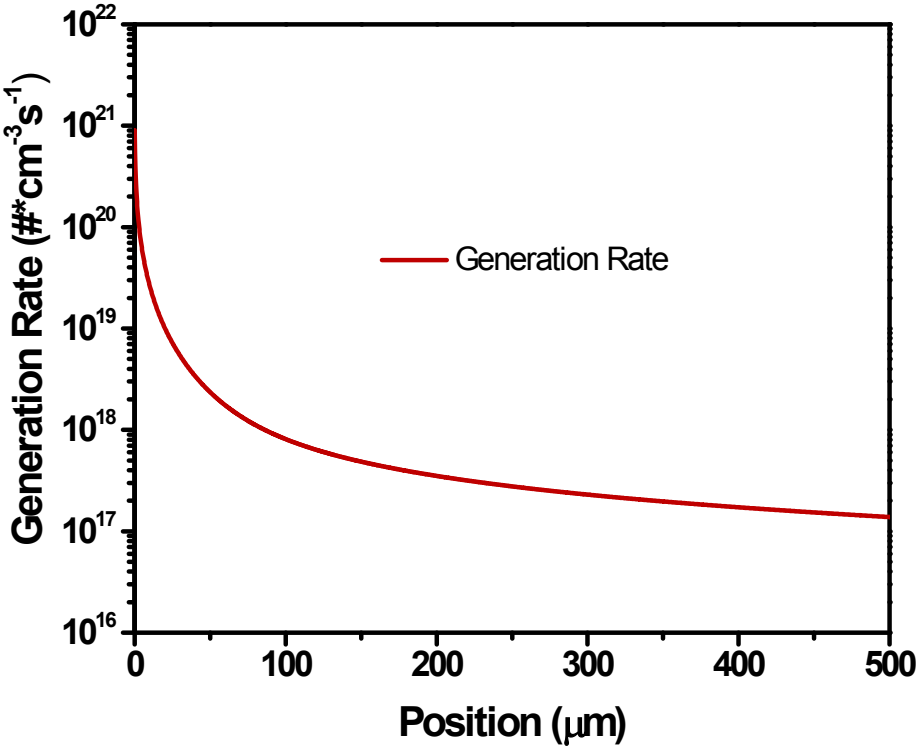


**Figure S1.** Charge carrier generation rate vs depth in the Si layer.

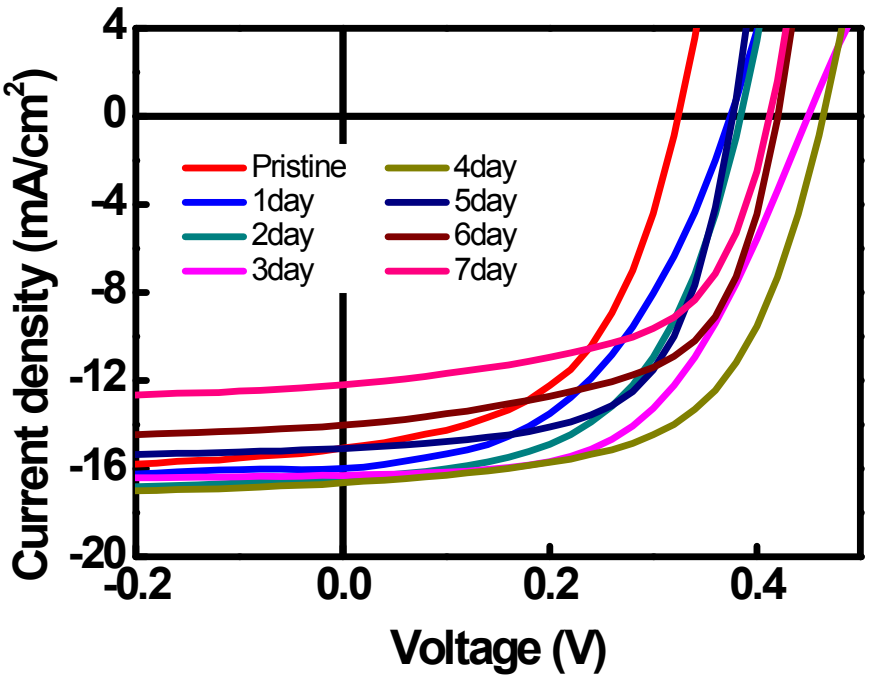


**Figure S2.** *J-V* Characteristics of *p*-Si and *p*-Si/$C_{60}$ hybrid solar cells with different $N_2$ aging time.

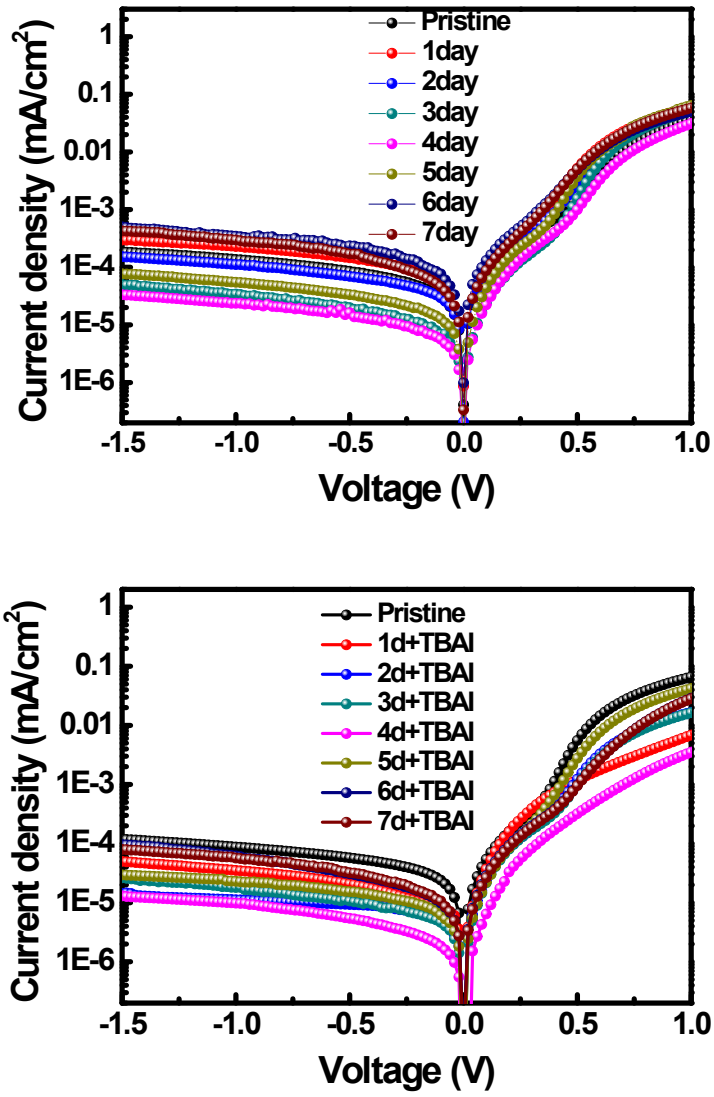


**Figure S3**. *J–V* characteristics in the dark of the hybrid solar cells with different aging times.

**Table S1**. Characteristics of *p*-Si/$C_{60}$ hybrid solar cells with 4day-aging and insertion TBAI

| **treatment** | $J_{SC}$ **(mA/cm²)** | $V_{OC}$ **(V)** | **FF** | **Eff. (%)** |
|---|---|---|---|---|
| Pristine | 15.80 | 0.43 | 0.55 | 3.68 |
| 1d+TBAI | 16.23 | 0.45 | 0.56 | 4.05 |
| 2d+TBAI | 16.56 | 0.49 | 0.58 | 4.70 |
| 3d+TBAI | 16.97 | 0.49 | 0.61 | 5.09 |
| 4d+TBAI | 19.10 | 0.50 | 0.60 | 5.67 |
| 5d+TBAI | 17.64 | 0.48 | 0.61 | 5.01 |
| 6d+TBAI | 15.88 | 0.44 | 0.59 | 4.17 |
| 7d+TBAI | 13.76 | 0.44 | 0.56 | 3.42 |

**Table S2.** Rs and Rsh of the hybrid solar cells with and without TBAI treatment

| | **Day** | **Pristine** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
|---|---|---|---|---|---|---|---|---|---|
| $R_S$ ($\Omega$-cm²) | Non | 5.58 | 3.77 | 3.11 | 2.88 | 2.63 | 2.63 | 3.63 | 3.97 |
| | TBAI | 4.76 | 3.60 | 2.98 | 2.81 | 1.09 | 1.61 | 5.06 | 5.20 |
| $R_{SH}$ ($\Omega$-cm²) | None | 925.9 | 1416.4 | 1715.2 | 5330.5 | 6535.9 | 3229.9 | 3030.3 | 1829.1 |
| | TBAI | 2386.6 | 4016.0 | 6369.4 | 7017.0 | 13568.5 | 8347.24 | 5224.3 | 5128.2 |

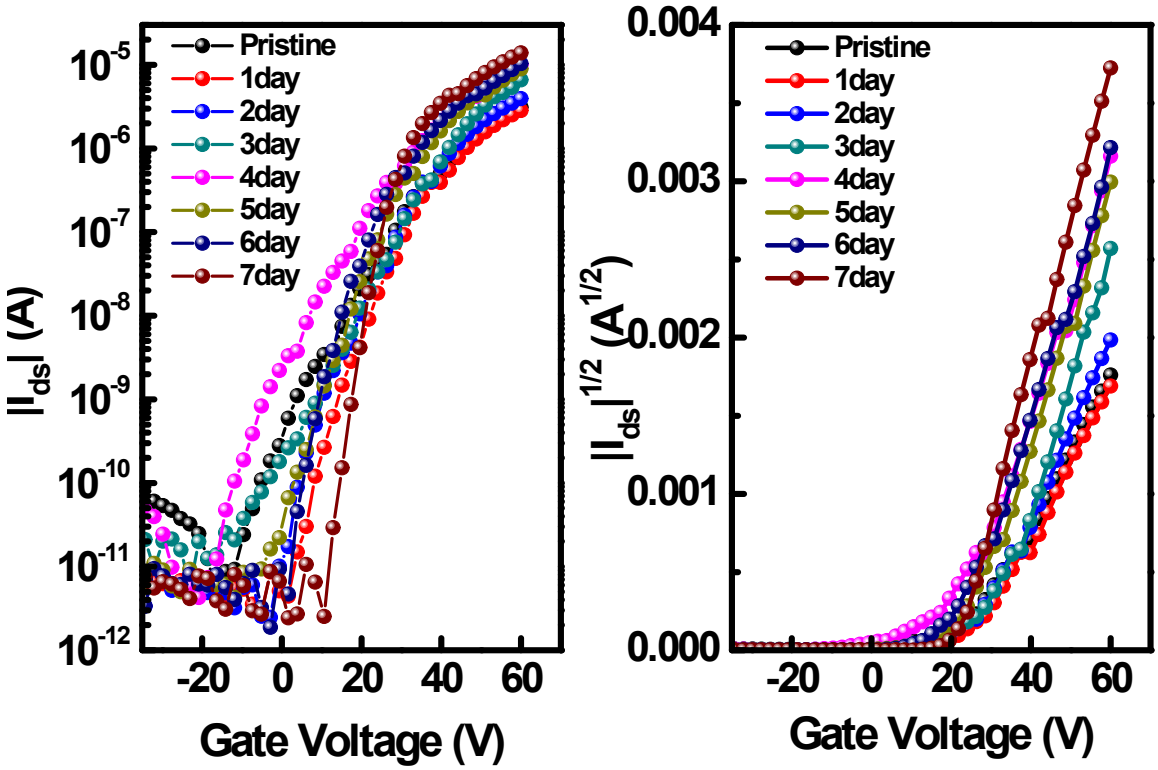


**Figure S4**. Transport characteristics of FETs fabricated using $C_{60}$ and $C_{60}$ with $N_2$ aging treatment.

**Table S3.** Built in potential, Carrier density and depletion width of different devices.

| day | treatment | $V_{bi}$ (V) | W [μm] | $N_a$ [$10^{15}$ $cm^{-3}$] |
|---|---|---|---|---|
| Pristine | - | 0.04 | 3.23 | 1.92 |
| | TBAI | 0.37 | 9.81 | 2.52 |
| 1 | - | 0.06 | 4.33 | 2.26 |
| | TBAI | 0.42 | 9.90 | 2.42 |
| 2 | - | 0.20 | 7.47 | 2.27 |
| | TBAI | 0.47 | 10.63 | 2.32 |
| 3 | - | 0.26 | 8.22 | 2.21 |
| | TBAI | 0.49 | 10.69 | 2.38 |
| 4 | - | 0.38 | 10.03 | 2.22 |
| | TBAI | 0.57 | 11.59 | 2.30 |
| 5 | - | 0.25 | 7.61 | 2.66 |
| | TBAI | 0.53 | 11.22 | 2.76 |
| 6 | - | 0.19 | 7.47 | 2.65 |
| | TBAI | 0.40 | 9.81 | 2.73 |
| 7 | - | 0.13 | 5.87 | 2.68 |
| | TBAI | 0.33 | 9.19 | 3.03 |

**Table S4.** FET characteristics of $C_{60}$ with different $N_2$ aging time**.**

| Aging time | Mobility ($cm^2s^{-1}V^{-1}$) | $I_{off}$ (A) | $I_{on}$ (A) | $I_{on}/I_{off}$ | $V_T$ (V) |
|---|---|---|---|---|---|
| Pristine | 0.00891 | 8.79E-12 | 3.11E-06 | 3.54E+05 | 21.4 |
| 1 day | 0.00927 | 7.45E-12 | 2.85E-06 | 3.82E+05 | 24.2 |
| 2 day | 0.0118 | 9.34E-12 | 3.94E-06 | 4.22E+05 | 26.2 |
| 3 day | 0.0302 | 3.40E-11 | 6.61E-06 | 1.95E+05 | 21.9 |
| 4 day | 0.0424 | 2.23E-11 | 9.98E-06 | 4.47E+05 | 11.48 |
| 5 day | 0.0328 | 8.57E-12 | 1.60E-05 | 1.87E+06 | 18.6 |
| 6 day | 0.0335 | 5.91E-12 | 1.03E-05 | 1.75E+06 | 16.45 |
| 7 day | 0.0350 | 4.12E-12 | 1.39E-05 | 3.37E+06 | 21.36 |

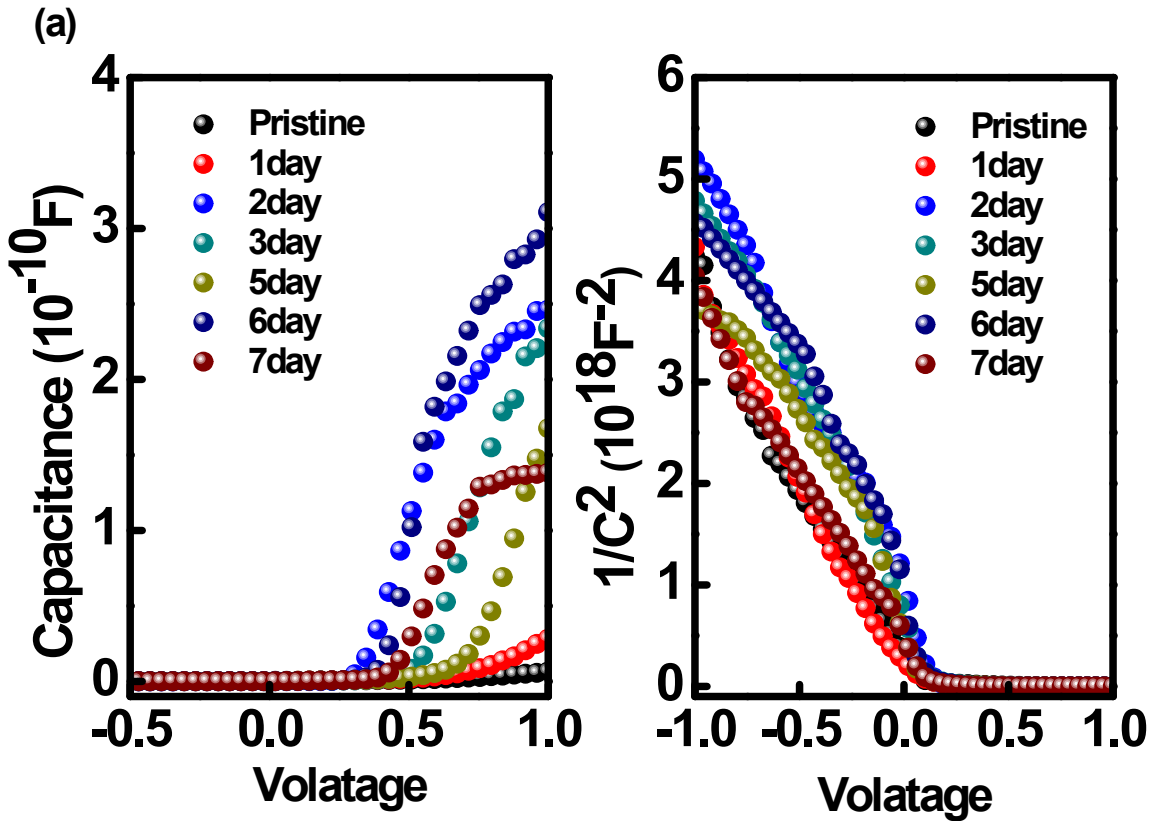


**Figure S5**. Capacitance-voltage and Mott-schottky-voltage characteristics of *p*-Si/$C_{60}$ hybrid device after days variable $N_2$ aging (a) without and (b) with insertion of a TBAI interfacial layer.

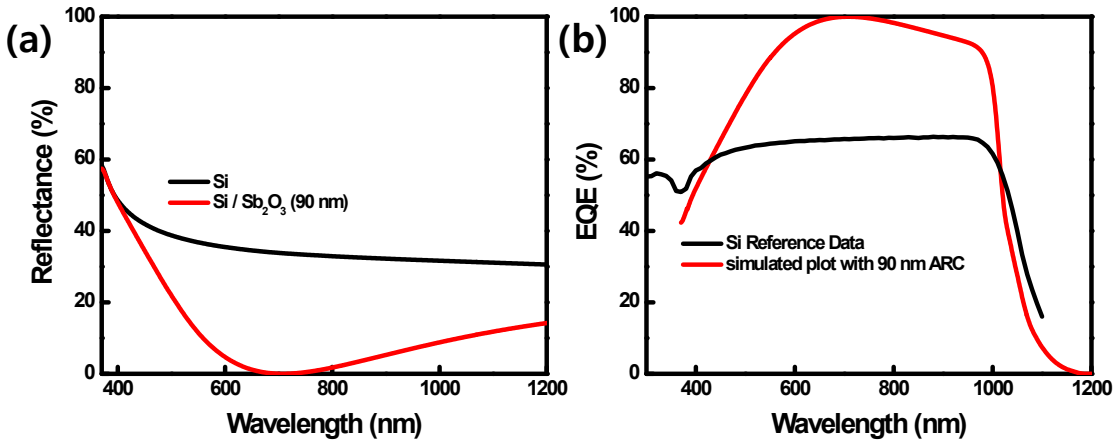


**Figure S6**. Simulated EQE data with 90 nm of $Sb_2O_3$ ARC layer.