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CdS-CdTe Heterojunction Nanotube Arrays for Efficient Solar Energy Conversion

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Supplementary images



Figure S1 SEM image of a CdTe tube grown by pulsed electrodeposition. Compared to the continuous deposition, lateral growth has minimized and tubes can be grown beyond the thickness of the polymer by pulsed deposition.



Figure S2 PXRD pattern of the electrodeposited CdTe layer before deposition of CdS layer. This pattern matched with the standard CdTe pattern [JCPDS 15-0770]. * indicates ITO peaks from the substrate.



Figure S3 SEM image of one nanotube pattern written in three different sizes to show the versatility of the protocol to fine tune the nanotube diameter and wall thickness without changing the feature size of the original pattern used in EBL. When the pattern is written in a larger area (a) the tube diameter as well as the distance between adjacent tubes (pitch) becomes larger and the tube wall thickness become thinner. When the same pattern is written in a small area (c) the tube pore diameter as well as pitch become smaller and thickness of the nanotube wall become larger.



Figure S4 XPS analysis of the CdTe nanotube arrays. (a) Binding energy spectrum of Te $3d_{3/2}$ and $3d_{5/2}$ (d) Binding energy spectrum of Cd $3d_{3/2}$ and $3d_{5/2}$ confirms the presence of CdTe.



Figure S5 Optical band gap determination of the (a) as-prepared nanotube arrays, (b) cadmium sulfide thin film and (c) CdS/CdTe nanotube combined device



Figure S6 Stability of the photocurrent response of the CdTe on CdS device under photoelectrochemical testing conditions. Initially, the device response was monitored by periodically turning on and off the light source. Then light source was kept on and photocurrent was recorded. It can be seen that the photocurrent response was stable for more than 2 h of continuous illumination.



Figure S7 Comparison of light on-off response of the CdTe nanotube array with CdS/CdTe nanotube arrays to see the effect of having a CdS layer. It was seen that there is ~25% increase of current density in the presence of n-type CdS layer.



Figure S8 Nyquist plots of (a) CdS/CdTe nanotube arrays (b) CdS/CdTe nanorod arrays and (c) CdS/CdTe thin film. The inset shows the equivalent circuit diagram.

CdTe morphology	R _s /ohm	R _{ct} /kohm	CPE/Fcm ⁻²
Nanotube array	0.28	15.02	5.80 x 10 ⁻²
Nanorod array	0.38	18.52	7.02 x 10 ⁻⁶
Thin film	0.44	819.10	1.65 x10 ⁻⁶

Table ST1 Evaluated EIS parameters of different geometries of the fabricated devices