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Supplementary Information

High-Performance Non-volatile Transistor Memories Using Amorphous Oxide Semiconductor and Ferroelectric Polymer

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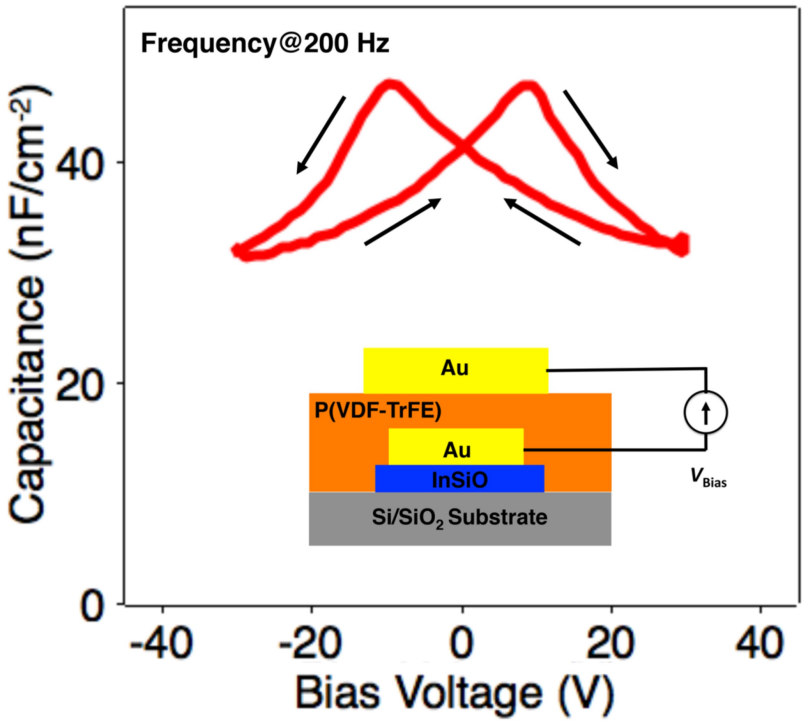

Figure S1. Capacitance versus bias voltage curve of an Au/P(VDF-TrFE)/Au sample. Inset shows the cross-sectional device structure. The capacitance was measured by applying a sweeping voltage (from −30 V to 30 V and then backward) at a low frequency of 200 Hz, exhibiting a typical butterfly shape. The capacitance represented the irreversible ferroelectric polarization, in which dipole switching occurs at the biased voltages of approximately 10 and −10 V.

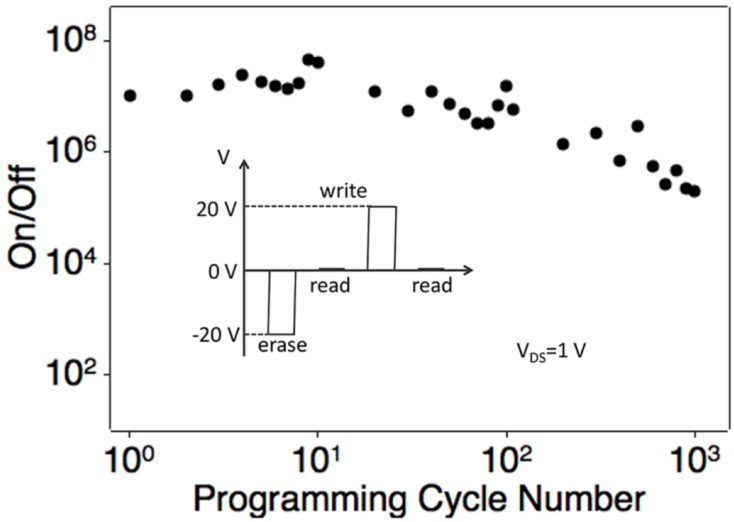

Figure S2. Programming cycle endurance obtained as the ratio of the on and off currents measured at the drain voltage of 1 V as a function of the number of programming cycles. The gate voltages for the write, read, and erase processes are set as 20 V, 0 V, and −20 V, respectively, as depicted in the inset.

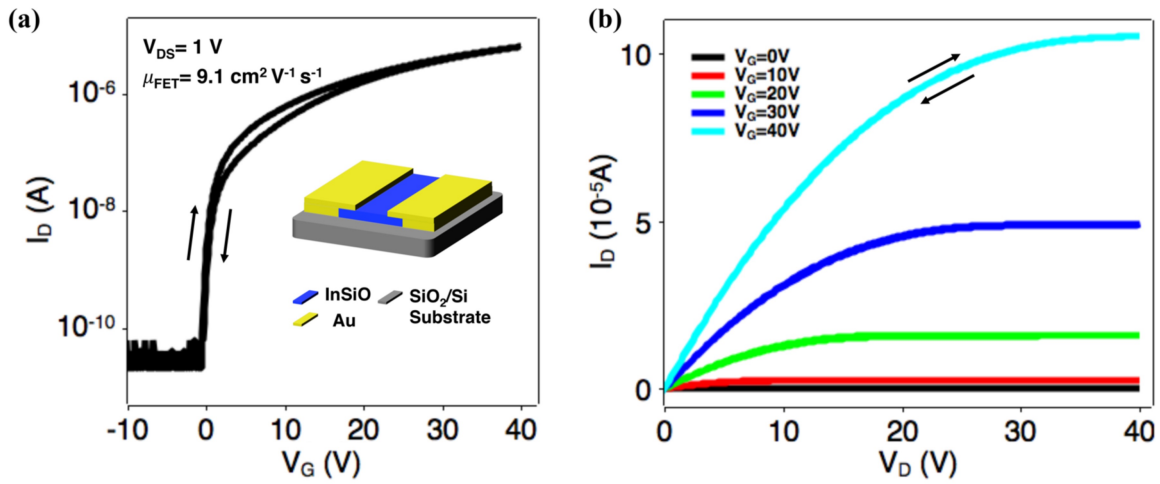

Figure S3. (a) Typical transfer and (b) output curves of bottom-gate device using SiO_2 as the dielectric and InSiO (In_2O_3:SiO_2 = 90:10 wt.%) as the semiconductor. Inset shows the device structure. A carrier mobility of 9.1 cm^2 V^{-1} s^{-1} was extracted.

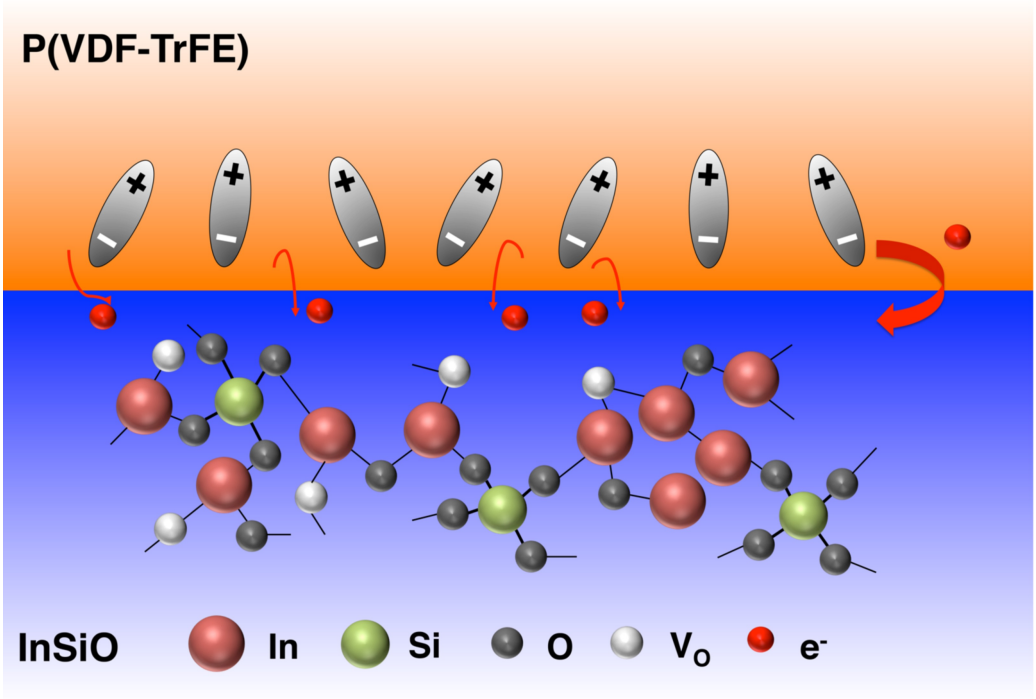

Figure S4. Schematic of the interfacial interaction between P(VDF-TrFE) and InSiO. The existence of interfacial charge transfer from the P(VDF-TrFE) layer to the semiconducting channel leads to the increase of charge carrier density, and then improves the carrier mobility. [1,2]

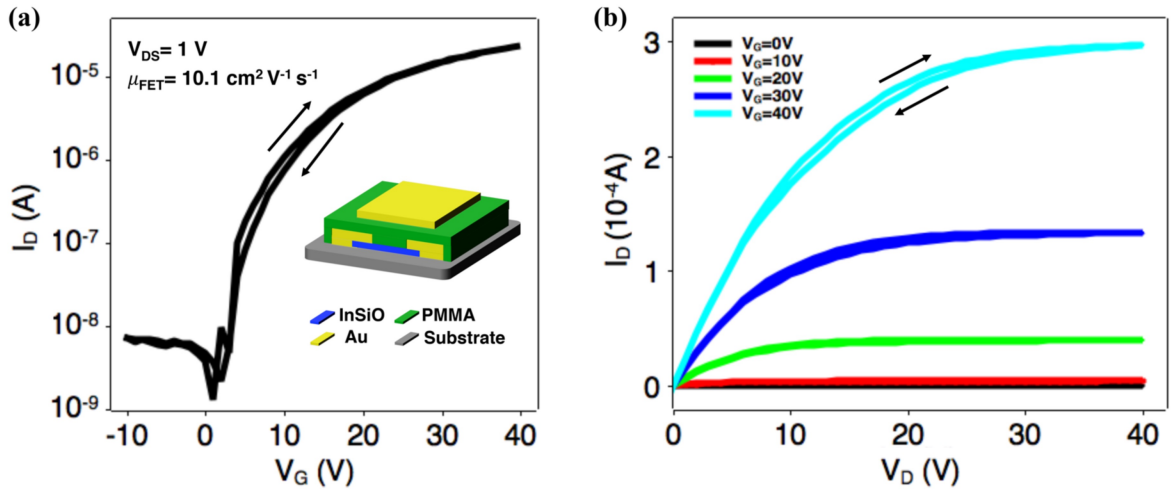

Figure S5. We fabricated the top-gate devices using poly(methyl methacrylate) (PMMA) as the top-gate dielectric and InSiO (In_2O_3:SiO_2 = 90:10 wt.%) as the semiconductor (inset). (a) A typical transfer exhibited the carrier mobility of 10.1 cm^2 V^{-1} s^{-1}. This value is similar with that of the FETs using SiO_2 as the bottom-gate dielectric, and both are significantly lower than that of devices using annealed P(VDF-TrFE). (b) Output curves of top-gate device using PMMA as dielectric.

Table S1. Carrier mobility, memory window and on/off ratio of the devices under different annealing condition of P(VDF-TrFE) film.

Annealing Temperature [°C]	μ_{FET}[a] [$cm^2 V^{-1} s^{-1}$]	μ_{FET}[b] [$cm^2 V^{-1} s^{-1}$]	Memory Window [V]	On/Off Ratio (V_G=0V)
Un-Annealing	0.02±0.01	0.79±0.59	6±1	$3.2\pm2.6\times10^2$
120	0.35±0.34	23.83±3.31	11±4	$2.1\pm1.5\times10^4$
125	17.12±7.38	47.87±8.34	14±2	$3.2\pm1.5\times10^5$
130	28.99±4.45	75.40±9.54	21±6	$0.9\pm0.3\times10^6$
140	0.44±0.49	27.90±5.42	4±2	$2.6\pm0.9\times10^3$

[a] The carrier mobility under quasi-static-frequency of 0.1 Hz for the capacitance measurements. [b] The carrier mobility under low-frequency of 200 Hz for the capacitance measurements.

References:

[1] M.-F. Lin, X. Gao, N. Mitoma, T. Kizu, W. Ou-Yang, S. Aikawa, T. Nabatame and K. Tsukagoshi, *AIP Adv.*, 2015, **5**, 017116.
[2] N. Mitoma, S. Aikawa, W. Ou-Yang, X. Gao, T. Kizu, M. F. Lin, A. Fujiwara, T. Nabatame and K. Tsukagoshi, *Appl. Phys. Lett.*, 2015, **106**, 042106.