Electronic Supplementary Information (ESI) for Energy & Environmental Science

Supporting Information

Monolithic perovskite-homojunction silicon tandem solar cell with over 22% efficiency

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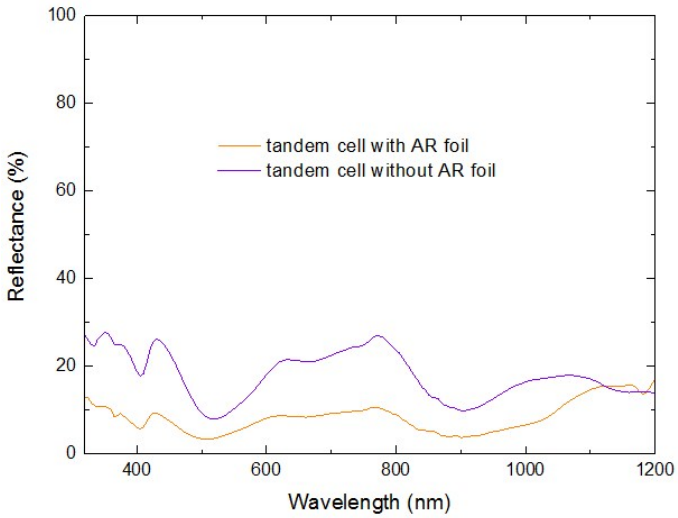

Fig. S1 Reflectance measurements for monolithic tandem cell with and without AR foil

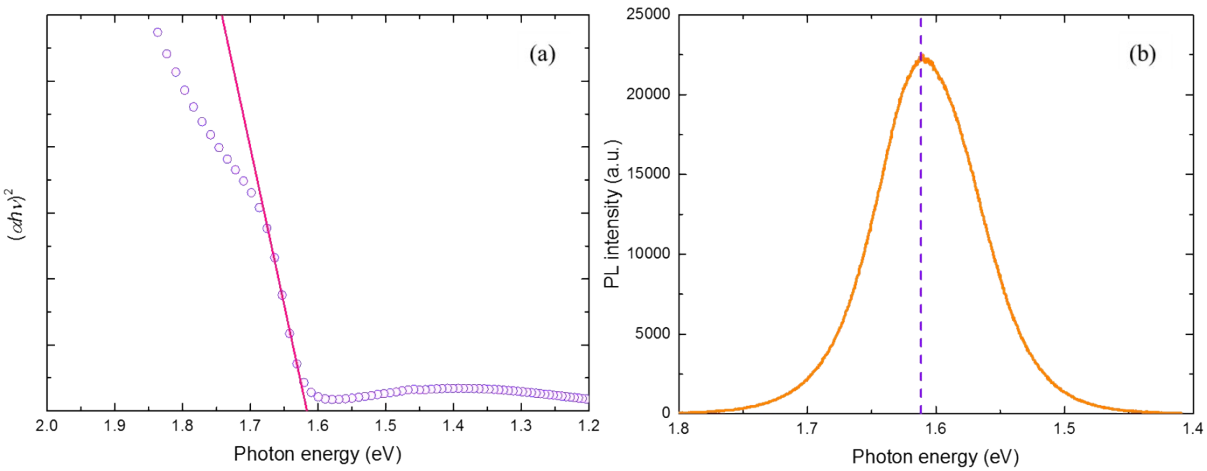

Fig. S2 $Cs_{0.07}Rb_{0.03}FA_{0.765}MA_{0.135}PbI_{2.55}Br_{0.45}$ quadruple cation perovskite with (a) Tauc plot where inset shows linear fit of the data at absorption onset to determine band gap energy (~1.62 eV). (b) PL spectrum where peak is at around ~1.62 eV.

Absorbed	Layers	Thickness	J_A (mA/cm^2)
Perovskite subcell	Textured silicone foil	450 μm	0.3040
	Front Au grid	120 nm	0.4688
	IZO	40 nm	0.8590
	MoO_x	10 nm	0.7280
	Spiro-OMeTAD	100 nm	2.700
	Quadruple Perovskite	300 nm	17.73
	Mesoporous-TiO_x	70 nm	0.000
	Compact-TiO_x	40 nm	0.000
	ITO	40 nm	1.091
c-Si subcell	SiN_x 2.9	50 nm	0.0895
	Al_2O_3	20 nm	0.000
	c-Si bulk (0.2% contact)	350 μm	17.70
	SiN_x 1.9	70 nm	0.005
	Ag	100 nm	1.300
	Al	800 nm	0.000

Table. S1 A list of absorption losses in the monolithic tandem device with optimised optical design. The simulation assumes 100% internal quantum efficiency for both top and bottom sub-cells, no photon recycling, and accurate measurements of refractive index (n) and extinction coefficient (k) of each layer in the tandem device.

	η_{eff} (%)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	R_s (Ω)
Prior annealing	14.9	661.1	30.2	74.6	1.272
Air 400 °C annealing (30 mins)	13.3	641.5	30.7	67.6	3.129
FG 400 °C annealing (60 mins)	14.3	635.3	30.7	73.2	1.863

Table. S2 Annealing test results for the bottom silicon cell in air and FG. The cells were measured using a Sinton flash tester, with fitted R_s using the Suns-V_{oc} method.

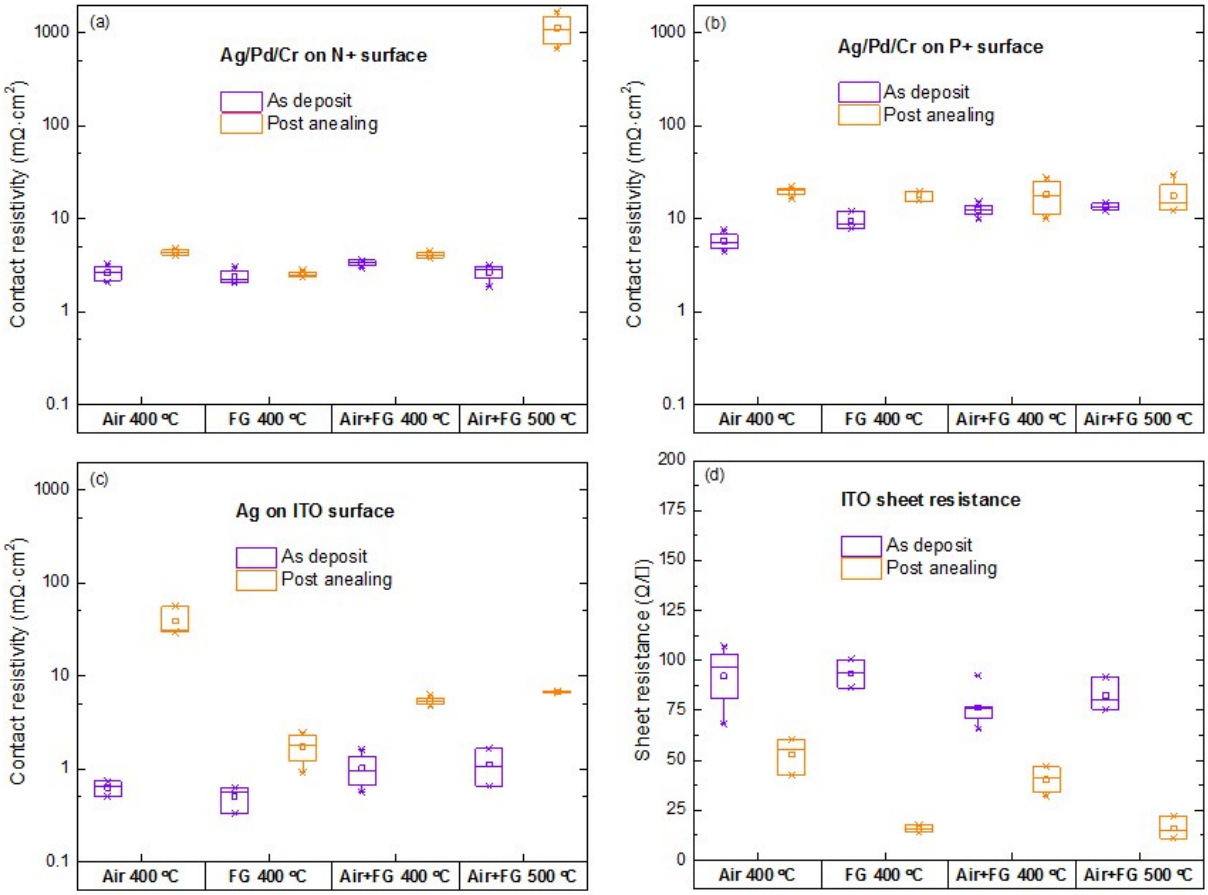

Fig. S3 Contact resistivity and sheet resistance of test samples both as deposites, and following annealing in Air/FG/Air+FG/ at 400 or 500 °C. Figures a-c show the contact resistivity between metal and diffused surfaces or ITO layer. Figure d shows the sheet resistance of the ITO layer under different annealing conditions.

When annealing at 400 °C, the contact resistivity of the metal - diffused silicon interfaces showed no obvious difference between air and forming gas (FG) annealing. The contact resistivity between Ag and ITO was observed to be high after an air anneal but can be sufficiently suppressed by annealing in forming gas, which is consistent with our cell result. We also attempted to anneal the structure at a higher temperature (500 °C) in air, but the IV scan showed non-ohmic behaviour for both TLM samples on diffused wafers. It showed clear evidence of the existence of Schottky barrier, and it may suggest a layer of oxide is formed at the interface. With air followed by FG annealing at 500 °C, the interface between POCL diffused silicon surface and Cr still shows a strong degradation while rest of the interfaces remain stable, and it suggests our current design of contact is not suitable for 500 °C annealing.

Generally, the sheet resistance of the sputter deposited ITO substrates is observed to decrease by about 50% following annealing at high temperature (400-500 °C), which is consistent with our cell results. Interestingly, we find that FG annealing can further reduce the sheet resistance to less than 20% of its as deposited value. In our current design, the current has to spread out from the metal contacts throughout the ITO layer, therefore a low sheet resistance is essential for a good FF. The reduction in sheet resistance upon forming gas annealing here raises an opportunity to further reduce the thickness of ITO layer to less than 40 nm and correspondingly reduce the absorption loss and increase the current output of the bottom c-Si cell.

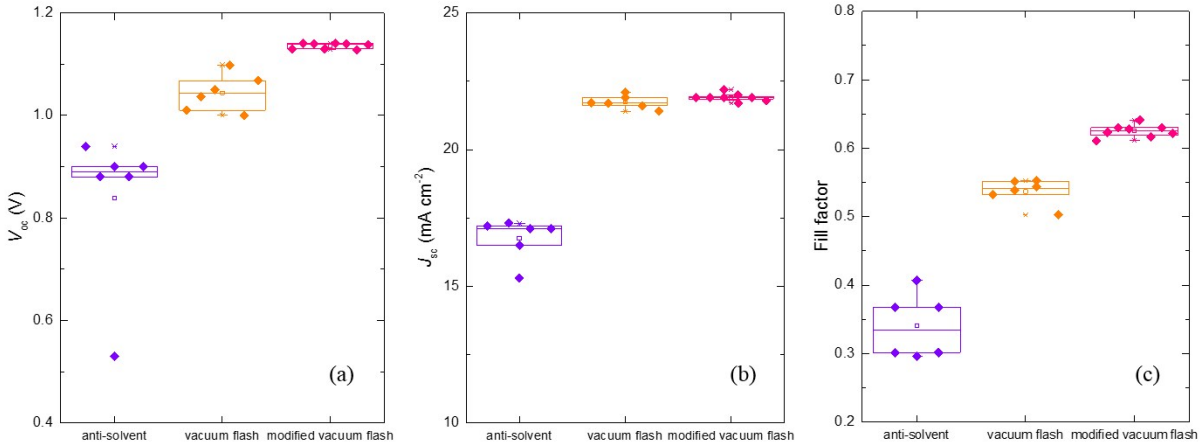

Fig. S4 Statistical distribution of the photovoltaic parameters for cells with different crystallization methods (2 step vacuum, 1 step vacuum and chlorobenzene anti-solvent method). All devices were tested at a 50 mV/s reverse scan rate.

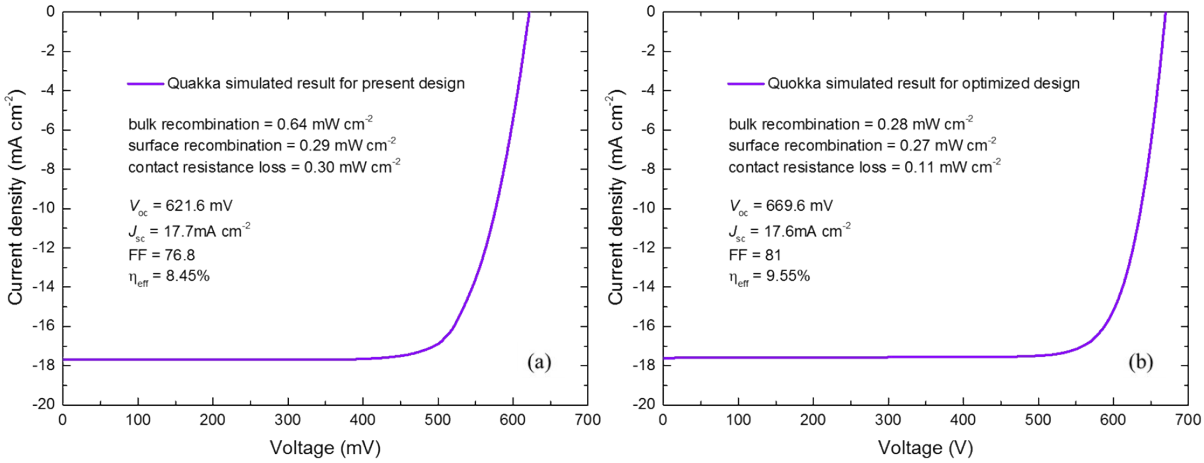

Fig. S5 *J-V* and loss analysis simulation done by Quokka for the c-Si subcell as in current design and future optimized design.

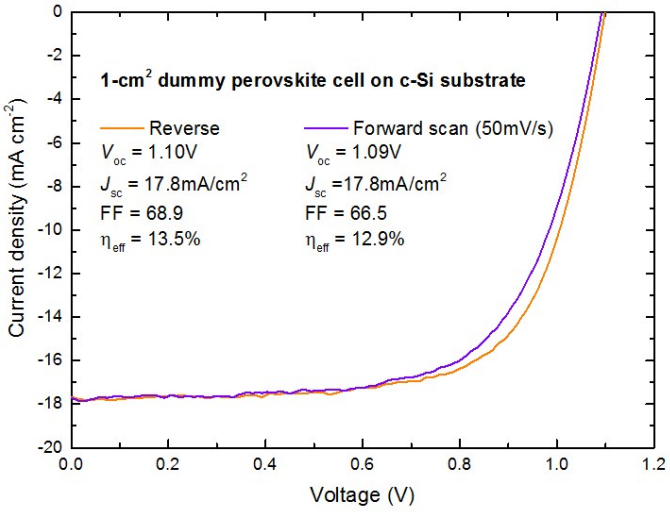

Fig. S6 *J-V* measurements of the dummy perovskite cell fabricated on a silicon substrate in the same way as for the monolithic 2-terminal tandem.