Electronic Supplementary Material (ESI) for Lab on a Chip.

Dynamic Monitoring of Transmembrane Potential Changes: Study of Ion Channels using Electrical Double Layer gated FET Biosensor

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Supplementary Information

EDL gated FET biosensor structure

The FET sensing region is defined as the gate electrode and channel openings (10x60 μm^2) separated by 65 μm which is filled by the test solution. Electrical double layer (EDL) is formed on gate electrode/solution and transistor dielectric/solution interfaces, as shown in Figure S1. When bias is applied to the gate electrode, applied potential drops across the test solution and the

transistor dielectric, because of the charge distribution in the EDL on the gate electrode and dielectric interfaces. This creates a solution capacitance C_s across the test solution (shown in Figure S1) which modulates the potential drop across the dielectric V_d.

The overall potential drop can be written as

$$V_g = \Delta V_s + \Delta V_d \qquad \text{Equation 1}$$

Where V_s and V_d refer to the potential drops across solution and transistor dielectric respectively, and V_g is the applied gate voltage.

Since impedance in an electrical circuit can be represented as

$$Z = \frac{1}{j\omega C} \qquad \text{Equation 2}$$

Where C is the total capacitance in the circuit, which can be written as

$$\frac{1}{C} = \frac{1}{C_S} + \frac{1}{C_d} \qquad \text{Equation 3}$$

Where C_s and C_d are the solution and dielectric capacitances respectively.

Hence V_d in equation 1 can be re-written in terms of solution capacitance as

$$\Delta V_d = \frac{\frac{1}{j\omega C_d}}{\frac{1}{j\omega C_d} + \frac{1}{j\omega C_s}} \times V_g = \frac{C_s}{C_d + C_s} \times V_g \qquad \text{Equation 4}$$

Where j and ω are current and angular frequency, respectively.

The potential drop across the dielectric eventually modulates the channel conductivity and hence the drain current of FET.

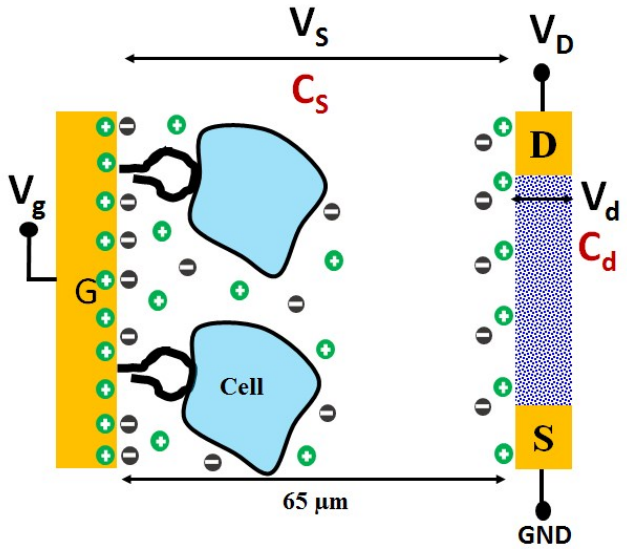

Figure S1 Schematic representation of potential drops across EDL gated FET biosensor.

Sensor measurement technique

The gate electrode separated from the FET channel region is supplied with a short duration (50 µs), pulsed gate voltage of amplitude 2 V. The applied potential profile is shown in Figure S2. During the first 2 µs of measurement, there is no V_g (gate bias) applied, following which V_g of 2 V is applied for 50 µs. During the measurement, a steady DC bias of 2.5 V is applied as drain voltage. The drain current response is also shown schematically in Figure S2, showing current gain calculations.

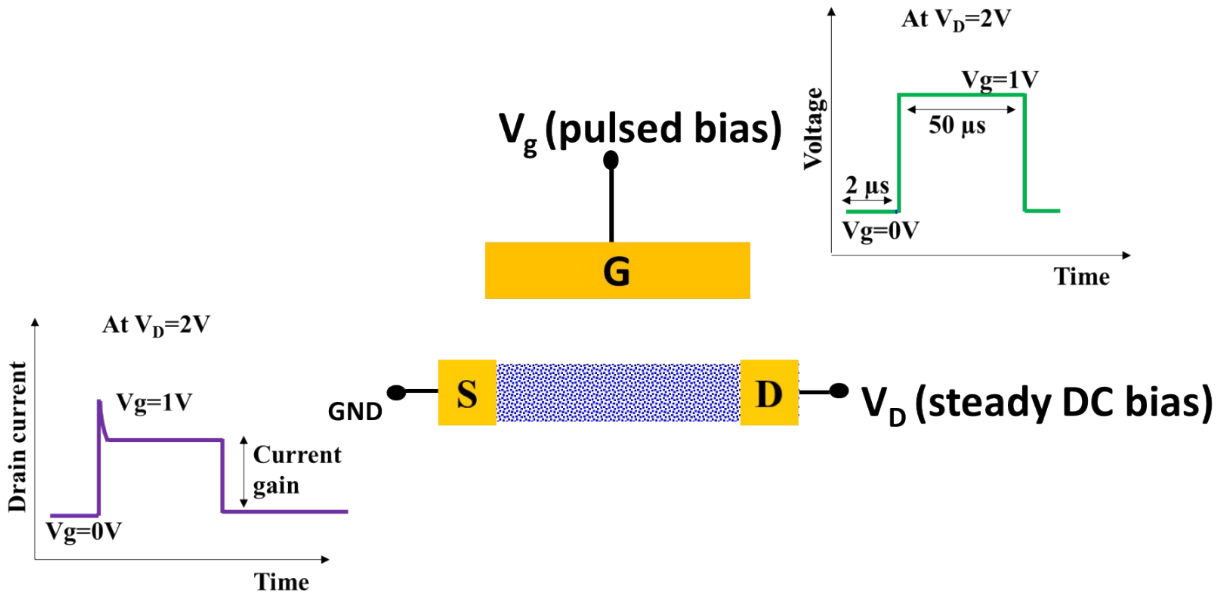

Figure S2 Sensor measurement parameters.