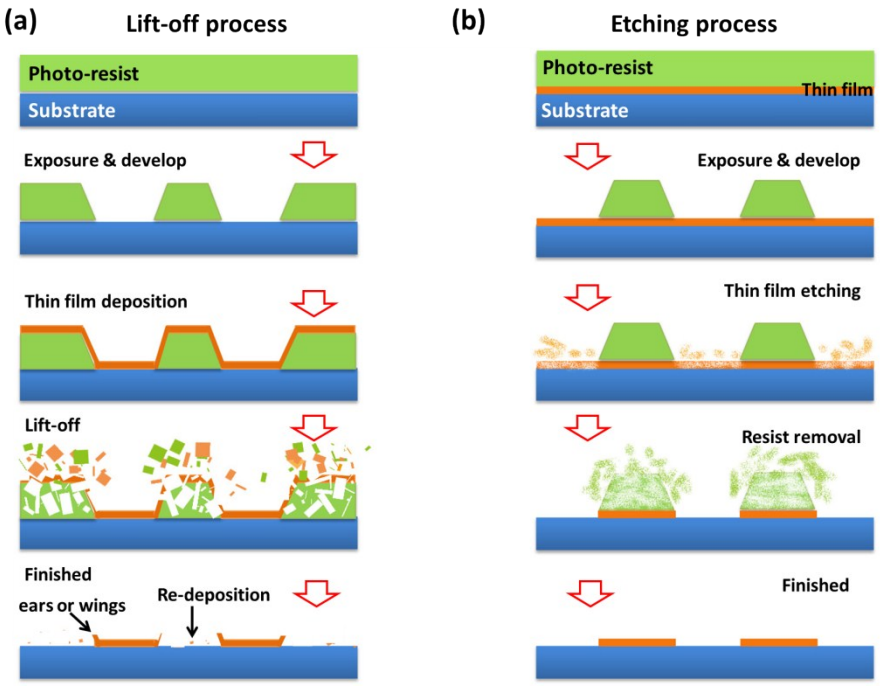
Electronic Supplementary Material (ESI) for Nanoscale.

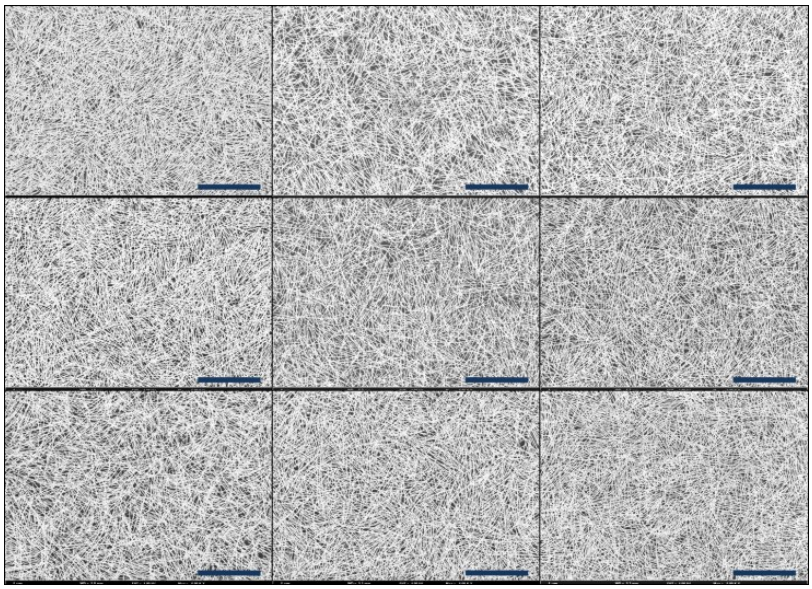
Supporting Information

S1 Schematic illustration of the lift-off and etching processes

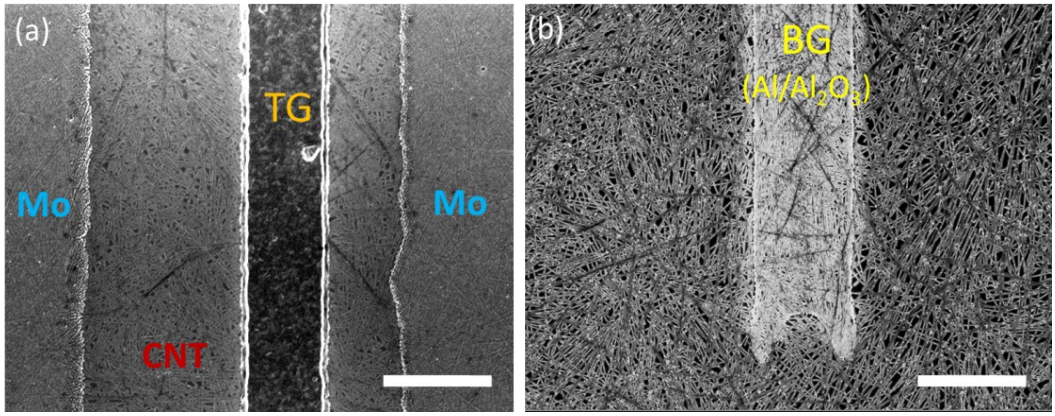


S2 SEM images of the CNT thin film deposited by surface deposition method

The SEM images were taken at nine evenly spaced locations of the 4-in wafer (scale bar: 5 μm). The results indicate the CNT thin film is clean and uniform around the wafer. The density of the CNT is about ~ 15 tubes/μm



The SEM image below shows the density of CNT deposited in the TG and BG devices are similar. Scale bar: 2 μm.



S3 Details of the etching process

We have 3 types of commercial available metal etchants for Al, Mo and Cu respectively in our lab, which are:

Al: Aluminum etchant type A (Al-etchant)

Mo: Moly etchant TFM (Mo-etchant)

Cu: Copper etchant APS-100 (Cu-etchant)

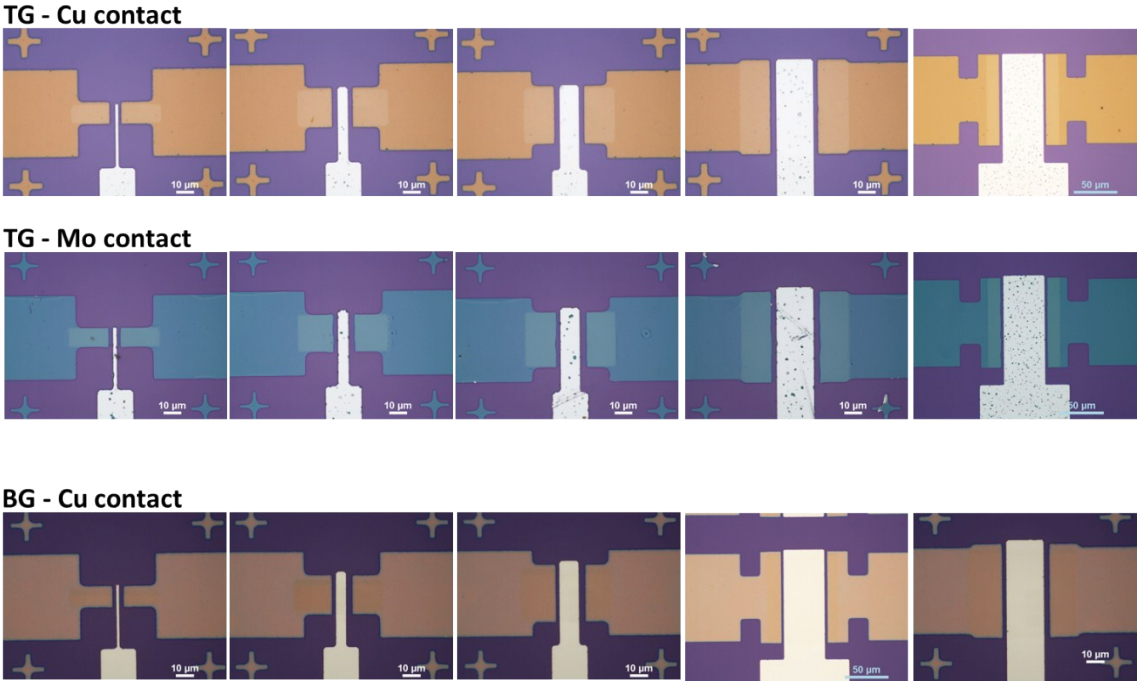
These etchants are purchased from Transene Company, Inc. From the Etchant/Metal compatibility chart supplied by Transene (transene.com) we know that Al_2O_3 will be etched by the Al-etchant with a much lower rate than Al. Cu is also etched by Al-etchant, while Cu-etchant does not etch Al. That is why the gate electrodes was firstly etched both in the TG and BG devices fabrication processes. No information of Y_2O_3 was given in the website of Transene, but our results demonstrate that it was etched by Al-etchant and Cu-etchant with relatively low rate, while not etched by Mo-etchant.

For TG device fabrication, the Al(100nm)/Y_2O_3(50nm) stack was etched by the Al etchant for 90 seconds. More than 80s was needed to clean the 100 nm Al layer vertically and the Y_2O_3 layer was cleaned in the leftover time (<10s). According to the lateral etching rate in Fig. 7 of the main text, the Y_2O_3 layer is about 300~400 nm narrower than the Al gate. The Cu layer was etched by Cu etchant for 5s. The Y_2O_3 layer was further etched a little bit laterally because Y_2O_3 was slightly etched by the

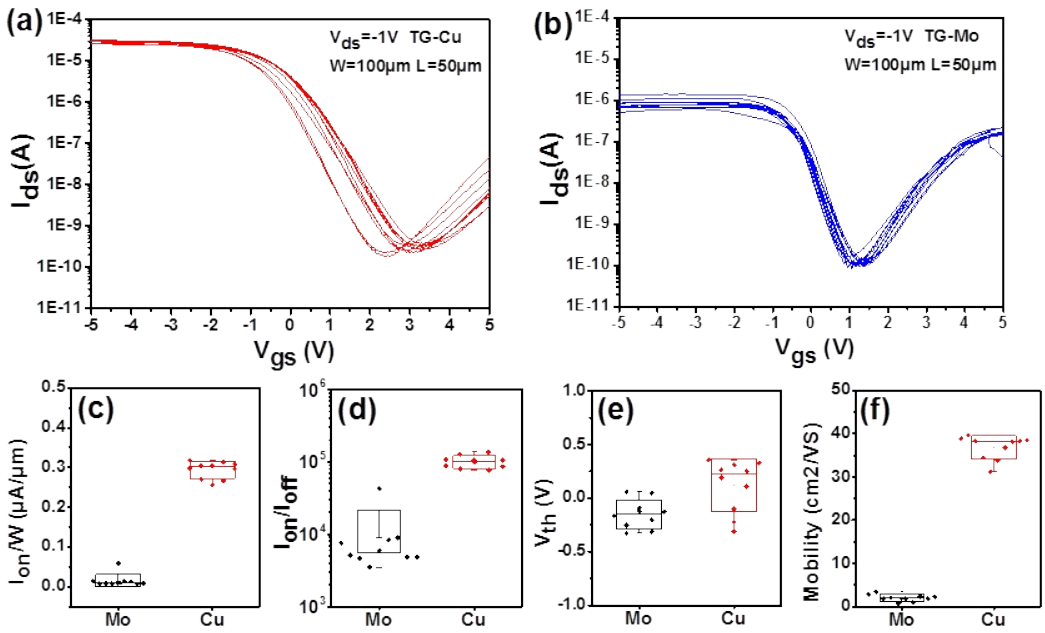
Cu etchant. The Mo layer was etched for 15s by the 20% diluted etchant. These layers were etched at 20°C.

For the BG device fabrication, the Al_2O_3(40 nm)/Al(40 nm) stack was etched by Al etchant for 120s at 50°C. According to the lateral etching rate at 50°C, narrower Al was obtained than the Al_2O_3. The Cu layer was etched by Cu etchant for 5s at 20°C.

S4 Images of the fabricated devices.

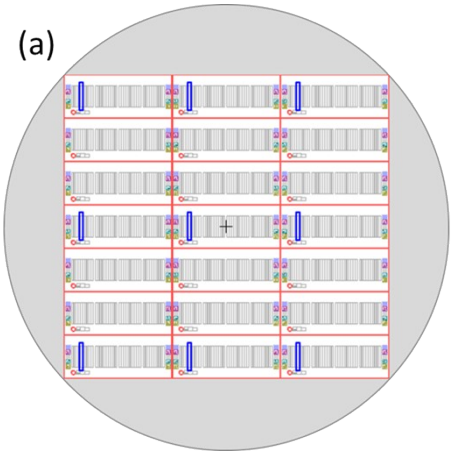


S5 Comparison of the Cu and Mo contacted TG devices.



Ten devices were measured for both Cu- and Mo-contacted devices with the same designed geometry (W = 100 μm, L = 50 μm). The Cu contacted devices show higher performances obviously.

S6 Performance uniformity of TG devices around large area



(b) I_{on} Average/Standard Deviation (μA)

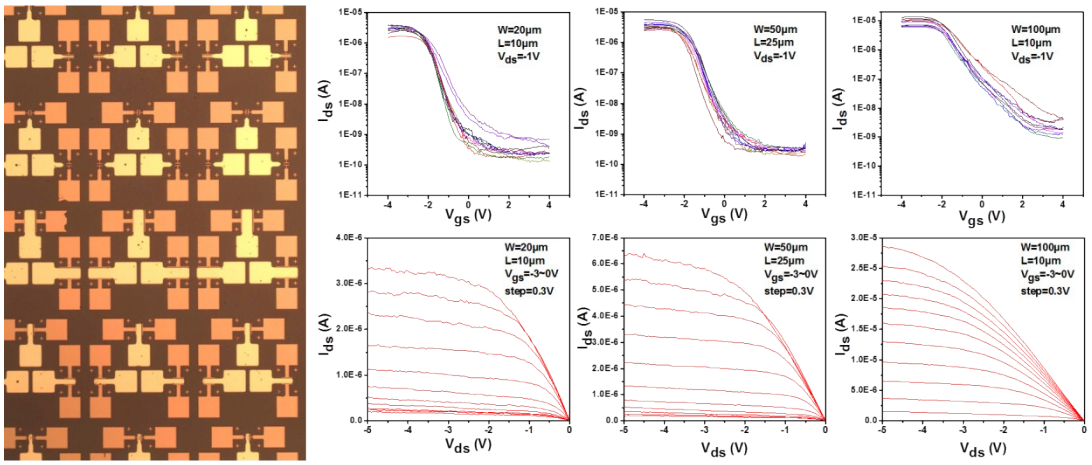
13.2 0.92	16.6 2.52	17.3 1.24
16.1 1.10	15.1 1.21	17.4 1.88
17.8 0.66	15.8 1.52	17.9 1.24

There are 21 dies, 7 rows by 3 columns, in the wafer. Each die includes four groups of devices. Each group has 100 units, 10 columns × 10 rows, and 3 devices in each unit. The devices have the same geometry, channel length (L), and width (W), in the same column, but different geometries for different columns. There are 10 designed

geometries which are classified to 3 different aspect ratios, i.e., W/L = 2 (with L = 5, 10, 15, 25, and 50 μm), W/L = 5 (with L = 5, 10, and 20 μm), and W/L = 10 (with L = 5 and 10 μm). The 90 devices with the same geometry, W=50μm and L=25μm, were selected from the row of (1, 4, 7) and group 1 of each column as shown by the blue rectangles in Fig. S6a, and 10 devices were measured in each blue rectangle. Fig. S6b shows the average and the standard deviation of the I_{on} of the ten devices.

S7 Fabrication of BG devices by direct deposition of Cu over the CNT thin film

The device fabrication process is similar to those of BG devices in Fig. 1b of the main text except for the fabrication sequence of the CNT channel and source/drain. After fabrication of the Al_2O_3/Al gate stack, CNT thin film was deposited and the channel was patterned by oxygen plasma. Then 60 nm Cu was sputtered all over the substrate. Afterwards, source/drain electrodes were defined by photolithography. The exposed Cu, including that covered the CNT channel, was etched by Cu etchant. Thus the entire CNT film, including the channel area of the device, experienced the bombardment of the sputtered Cu atoms. Fig. S7 shows optical image of the fabricated devices and typical electrical property measurement results.



S8 Etching of Y_2O_3 over the CNT thin film

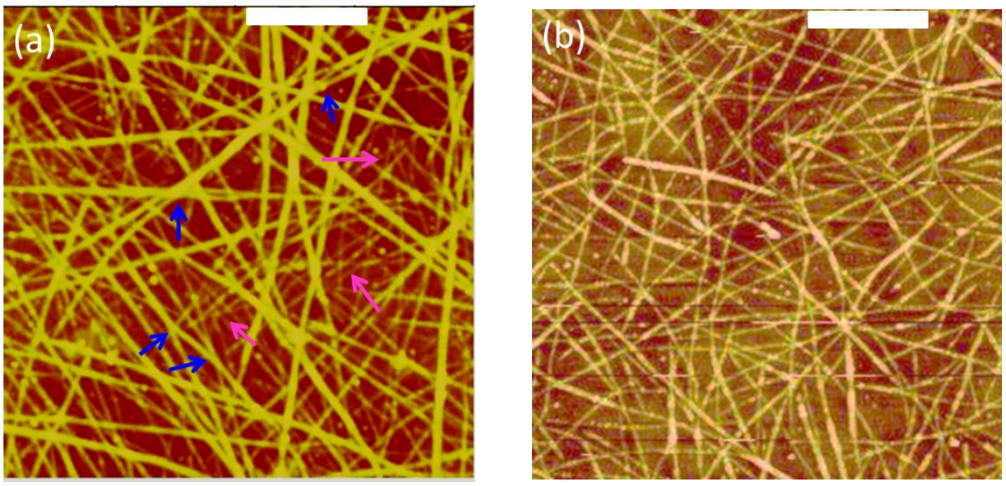
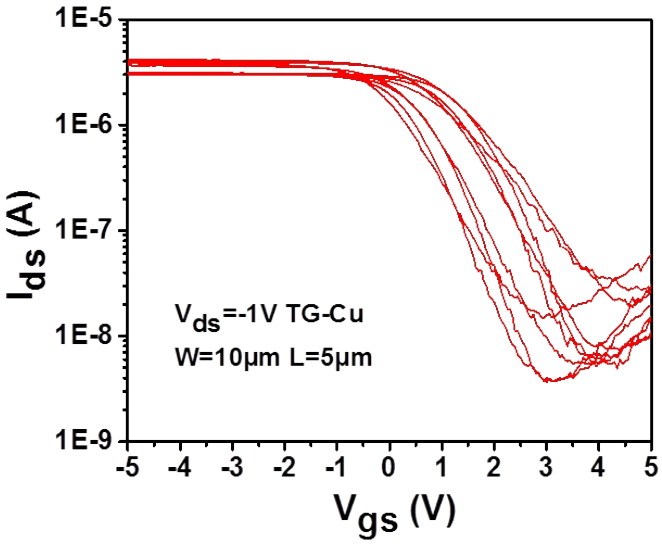
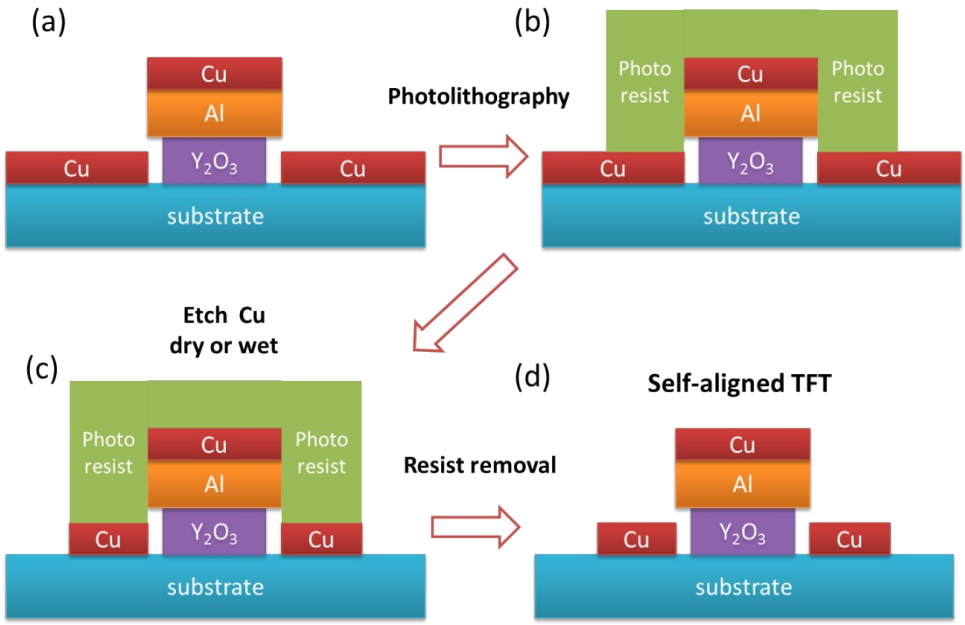


Fig. S8(a) is an AFM image taken at the gap area of a TG device (Fig. 7 of the main text). The covered Y_2O_3 layer was etched by the Al etchant for ~10s. (b) is taken from the channel area of a device fabricated by usual lift-off process. Scale bar: 0.5μm. The thicker tubes appeared in (a) are mainly bundles which are easily recognized as pointed by the blue arrows. The individual single tubes are marked by the magenta arrows. By comparing these images we can concluded that the Y_2O_3 layer in (a) was removed cleanly.

S9 Transfer curves of more short channel length devices.



S10 Suggested fabrication process for very small size CNT-TFTs



The suggested fabrication process for small channel length device is similar to the TG device fabrication in Fig. 1a of the main text. After the Al/Y_2O_3 gate stack etching, Cu was deposited to the substrate entirely as shown in Fig. S10(a). Then S/D were patterned as shown in (b)-(d). The gap between the gate and S/D electrode (as shown in Fig. 7a of the main text) was minimized by a self-align deposition due to the undercut profile of the gate stack.