Supplementary Information to "Nonvolatile reconfigurable sequential logic in HfO_2 resistive random access memory array"

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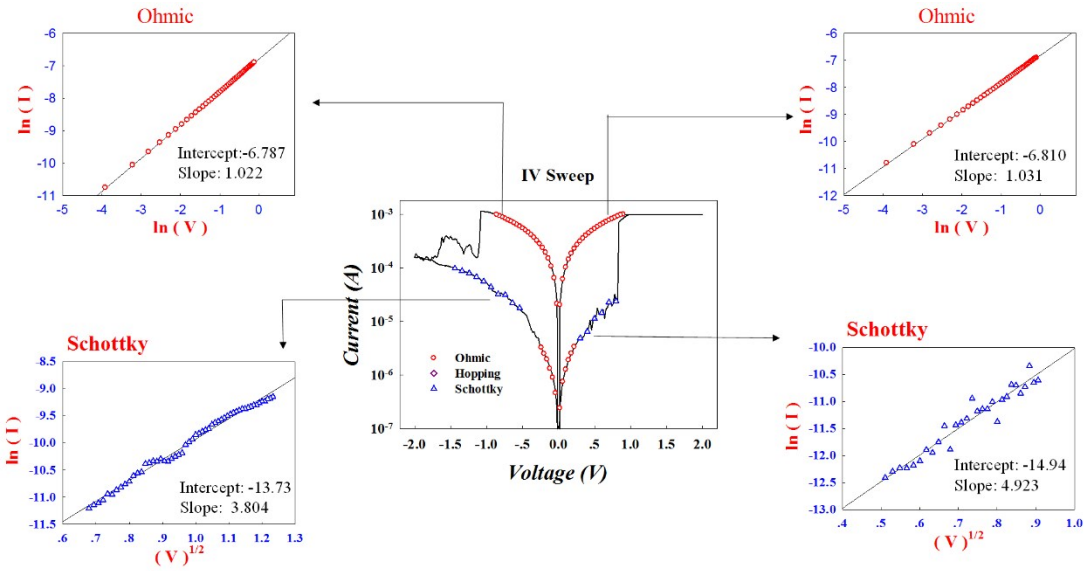

Fig. S1 Conduction mechanism analysis of the HfO_2 RRAM through *I*-*V* characteristics fitting. By drawing the curve of Ln(*V*)-Ln(*I*), the slope of the curves can be obtained as 1.022 and 1.031 in LRS under negative and positive sweeping, respectively, which means the conduction mechanism is dominated by Ohmic mechanism in LRS. By drawing the curve of $(V)^{1/2}$-Ln(*I*), we can found that the slopes of the curves under negative and positive sweeping in HRS is different (3.804 and 4.923, respectively), which means the conduction mechanism is dominated by Schottky conduction caused by different electrode of the RRAM device in HRS.

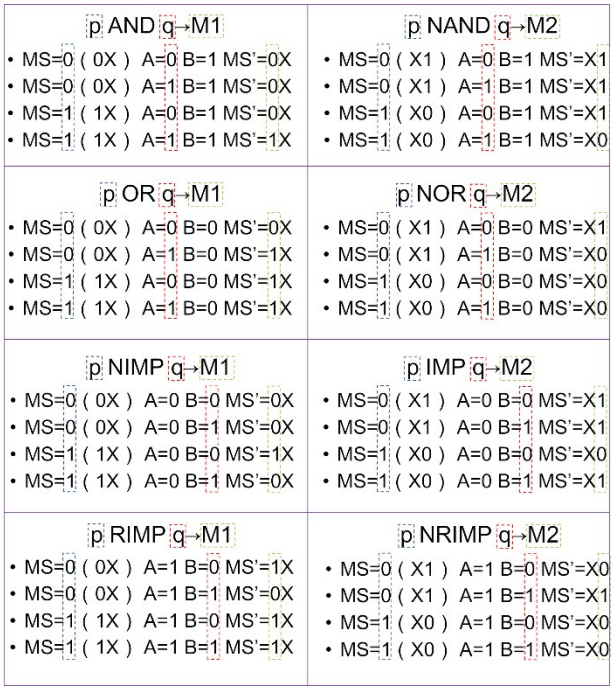

Fig. S2 Parameter assignments of the 8 different Boolean logic functions. The variables *p* and *q* are assigned as shown in the blue and red dot blocks, respectively. The logic results are stored as shown in the green dot blocks. i) AND and NAND logic can be achieved by assigning *p*, *q* and 1 to S, A and B, respectively. The results are stored in M_1 and M_2, respectively. ii) OR and NOR logic can be achieved by assigning *p*, *q* and 0 to S, A and B, respectively. The results are stored in M_1 and M_2, respectively. iii) NIMP and IMP logic can be achieved by assigning *p*, 0 and *q* to S, A and B, respectively. The results are stored in M_1 and M_2, respectively. iv) NIMP and IMP logic can be achieved by assigning *p*, 1 and *q* to S, A and B, respectively. The results are stored in M_1 and M_2, respectively.

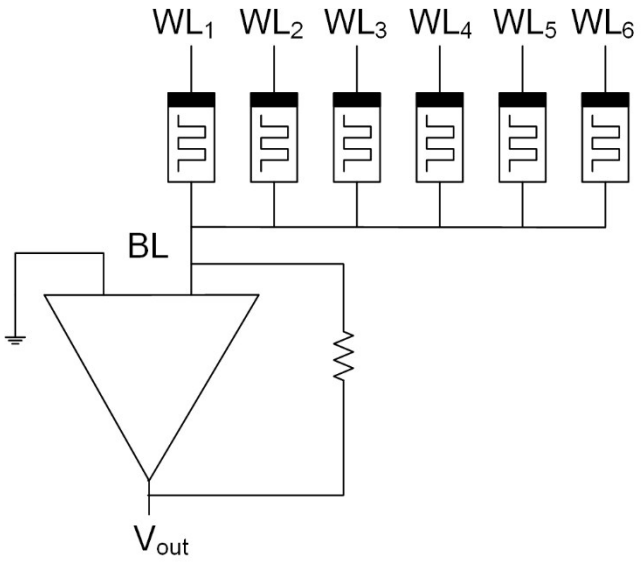

Fig. S3 The readout of logic result. The logic results stored in the RRAM devices can be acquired by applying a read voltage V_{read} to the selected unit. Through the operational amplifier, a current signal flowing through the RRAM is converted to a voltage signal, hence the logic results can be read out.

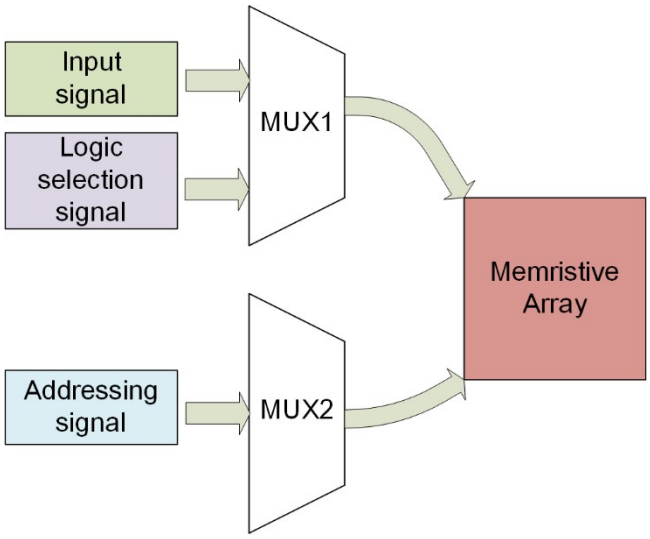

Fig. S4 Circuit architecture for the RRAM computing architecture. Reconfigurable logic operation can be programed by this circuit architecture. Through MUX1, the performed logic function can be selected by logic selection signal, then the input signal can be applied to the selected units through MUX2 controlled by the addressing signal.