Supporting Information for

Vertical resonant tunneling transistors with molecular quantum dots for large-scale integration

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1. Estimation of number density of molecules deposited on SiO_2 surface

The number density and surface distribution of the molecules on the SiO_2 surface were estimated by scanning tunneling microscopy (STM). Fig. S1 shows a typical STM image of C_{60} molecules on an atomically resolved Si (111) 7×7 surface. The deposition conditions were the same as those for the formation process of the vertical resonant tunnel transistors. We assumed here that the molecules were distributed in a similar manner on the SiO_2 surfaces, as the molecules are assumed to be immobile on both surfaces. Individual molecules were observable, and were isolated from each other on the Si (111) 7×7 surface. Therefore, the energy levels of individual molecules are responsible for the observed resonant tunneling, despite the fact that many molecules are placed on the SiO_2 layer. The number density of molecules was estimated to be 10^{12}-10^{13} cm^{-2}, indicating 10^4-10^5 molecules would be embedded in a transistor.[S1]

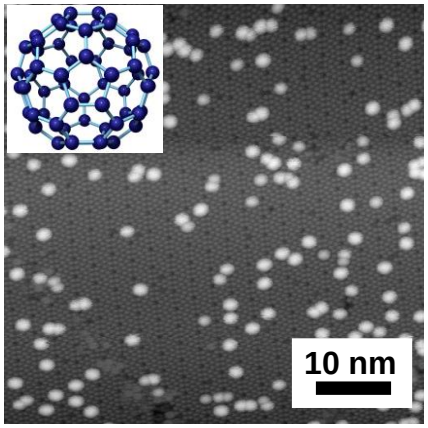

Fig. S1 A scanning microscopy image of C_{60} molecules deposited on a Si (111) (7×7) substrate.

2. Resonant tunneling in a well-defined double tunnel junction formed by electron-beam lithography

Figs. S2a and S2b show the current (*I*)-voltage (*V*) and d*I*/d*V* curves in the microfabricated tunneling junctions, to confirm the resonant tunneling through C_{60} molecules. The measurement temperature was fixed at 20 K. The tunnel junction consisted of an Au/Al_2O_3/C_{60}/SiO_2/p-type Si substrate. The thickness of the insulating layers was 2 nm for the SiO_2 layer and 3 nm for the Al_2O_3 layer, based on x-ray refractivity and transmission electron microscopy measurements. The width and length of the double tunnel junctions were 60 nm and 100 μm, respectively (see inset in Fig. S2a). Multiple staircases were clearly observable in the negative voltage in the *I*-*V* curve for a sample with p-type Si substrate (Fig. S2a); the four peaks in the d*I*/d*V* curve, as illustrated by the red arrows, were observed at the subsequent voltages of -1.1, -1.3, -1.4, and -1.5 V (Fig. S2b). The observed peak positions in the d*I*/d*V* curves can identify the split highest occupied molecular orbitals (HOMOs) of C_{60} molecules. Here, the split levels are depicted as HOMO, HOMO -1, HOMO -2, and HOMO -3. The splitting of the molecular orbitals is well known to occur through molecular distortion, although the molecular orbitals are highly degenerated due to the symmetric structure.[S2] The assignment is also supported by the reported results of scanning tunneling spectroscopy measurements[S3,S4] and those of our previous study.[S1].

Meanwhile, a triple staircase was observed in the positive voltage in the *I-V* curve for a sample with n-type Si substrate (Fig. S2c). The three peaks in the d*I*/d*V* curve were visible at 0.5, 0.8, and 1.0 V (Fig. S2d). The peak locations coincided with those of the lowest unoccupied molecular orbitals (LUMOs), which are noted as LUMO, LUMO +1, and LUMO +2. These results prove that the molecules were not destroyed throughout all the lithography processes.

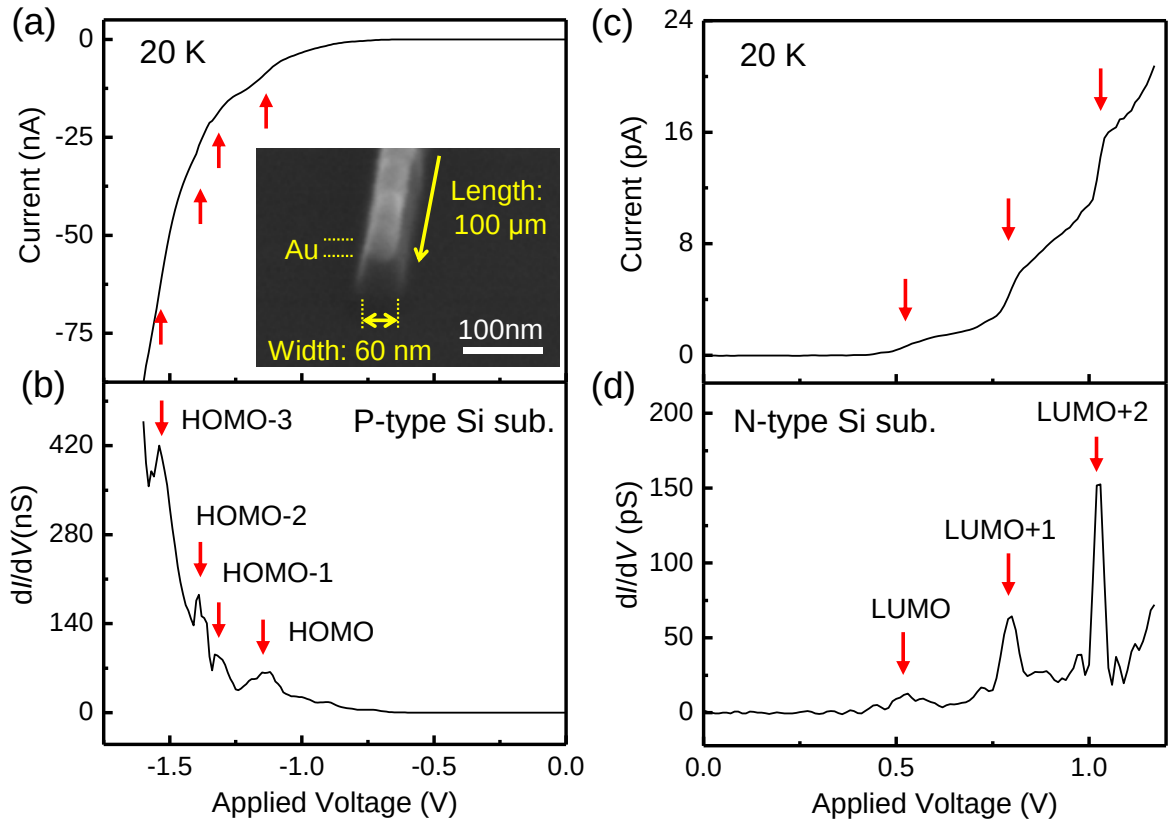

Fig. S2 Resonant tunneling via molecular dots in defined double tunnel junctions. (a) An *I-V* characteristic and (b) a d*I*/d*V* curve of a sample with p-type Si substrate. The inset in (a) shows a scanning microscopy image of the double tunnel junction formed by EB lithography. (c) An *I-V* characteristic and (d) a d*I*/d*V* curve of a sample with n-type Si substrate.

3. Formation process of vertical resonant tunneling transistor

The vertical transistor configuration was formed using standard electron-beam (EB) lithography and reactive-ion etching (RIE). The processes are illustrated in Fig. S3. First, a Au electrode was patterned by EB lithography on a uniform Al_2O_3 layer. Then, the sample was

etched by RIE with trifluoromethane (CHF_3), to form the one-dimensional mesa structure. Here, the Au top electrode worked as a hard mask in the etching process. Then, a 30 nm-thick Al_2O_3 film was grown as a gate insulator on the tunnel junction, using an atomic layer deposition method. The temperature was fixed at 130 ºC. As a result, 100 nm-thick Au films, which acted as a gate electrode, were patterned by EB lithography.

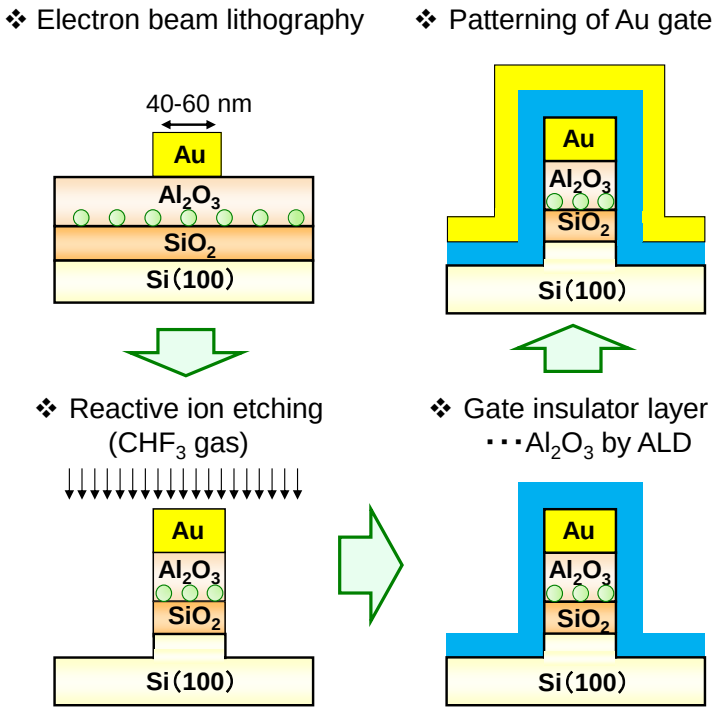

Fig. S3 Formation process of a vertical resonant tunneling transistor.

4. Gate voltage dependence of peak shifts in differential conductance curves and capacitance between source and gate electrodes

Figure S4 shows the gate voltage dependence of dI_d/dV_d peak shifts assigned to unoccupied molecular orbitals. As a comparison, the variation of capacitance between source and gate electrodes is plotted in the same figure. Here, the individual peak shift was calculated from those of Figure 3d in the manuscript; the amplitude of peak shifts was normalized by initial peak positions in the dI_d/dV_d curve without gate voltage. The amount of peak shifts for gate voltage is closely related to the reduction of capacitance between source and gate electrodes, which support that the peak shifts in dI_d/dV_d curves were induced by formation of depletion layers in Si substrates.

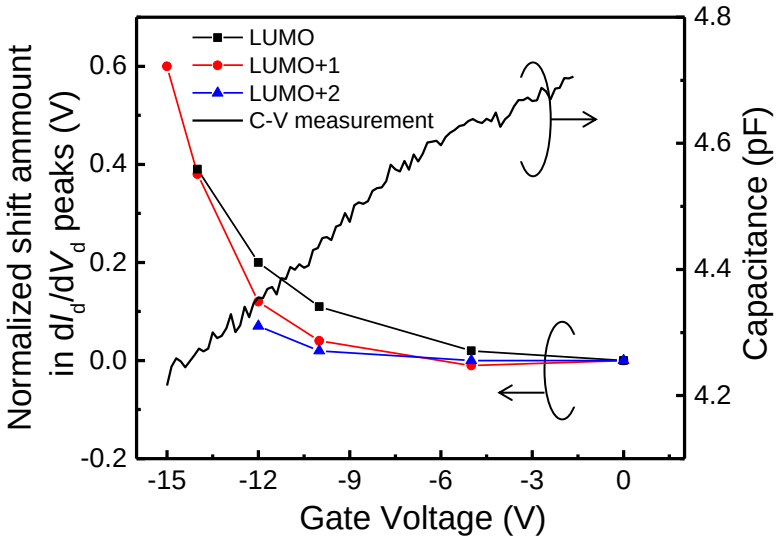

Fig. S4 Gate voltage dependence of capacitance between gate and source electrodes and the amount of peak shifts on unoccupied molecular orbitals.

References

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