

Supporting Information

A Novel Artificial Synapse with Dual Modes using Bilayer Graphene as the Bottom Electrode

He Tian,^{1, †, *} Wentian Mi,^{1, †} Haiming Zhao,¹ Mohammad Ali Mohammad,^{1, 3} Yi Yang,¹ Po-Wen Chiu,² Tian-Ling Ren^{1*}

¹Institute of Microelectronics and Tsinghua National Laboratory for Information Science and Technology (TNList), Tsinghua University, Beijing 100084, China

²Department of Electrical Engineering National Tsing Hua University, Hsinchu 30013, Taiwan

³School of Chemical and Materials Engineering (SCME), National University of Sciences and Technology (NUST), Sector H-12, Islamabad 44000, Pakistan

[†] These authors contributed equally to this work.

*Email: tianhe10@tsinghua.org.cn, RenTL@tsinghua.edu.cn

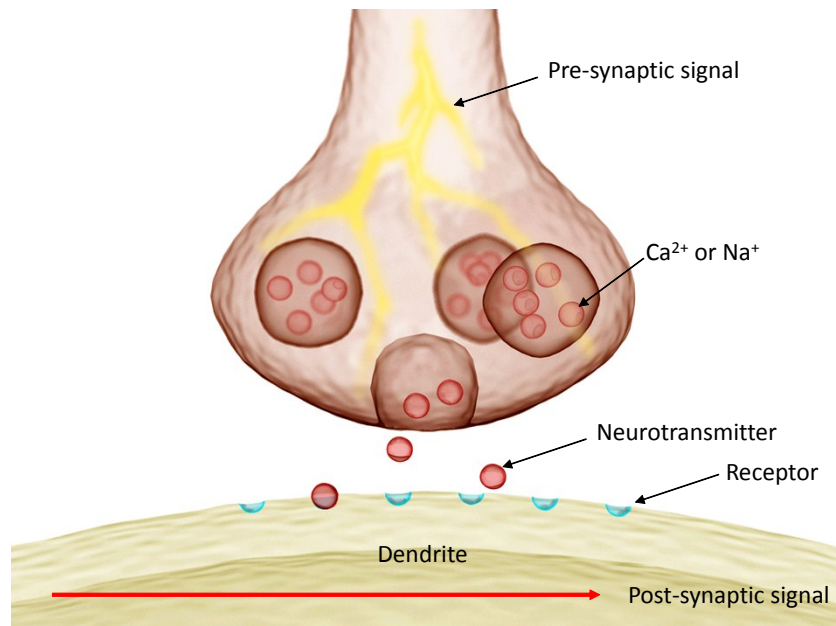


Figure S1. Schematic image of a biological synapse, which assists in the visualization of the three-terminal synaptic device configuration.

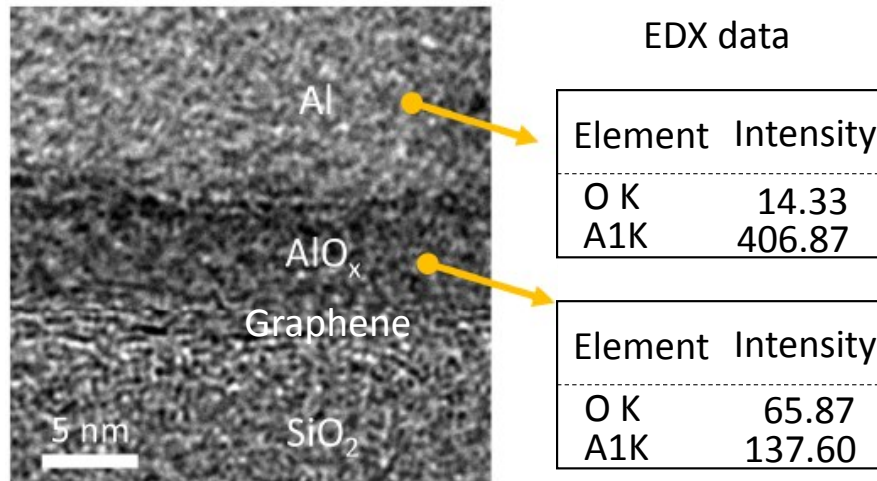


Figure S2. A TEM image showing a cross-section of the Al/AIO_x/graphene multilayer on SiO₂. The elemental composition information of the Al and AlO_x layers are also included.

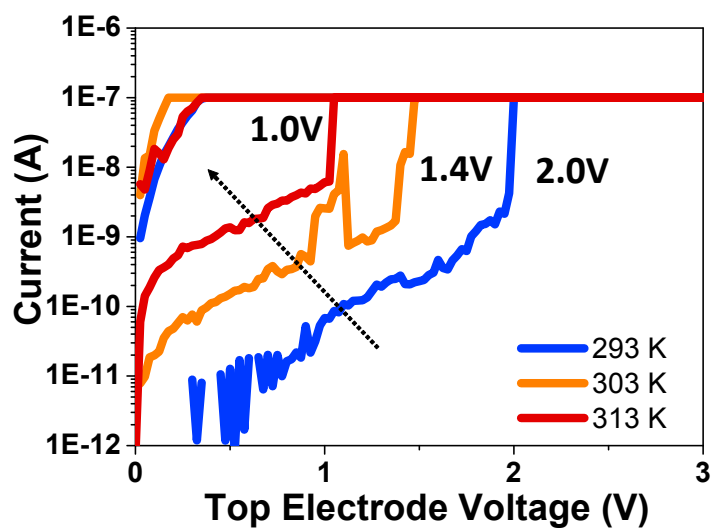


Figure S3. Switching cycles for the Al/AlO_x/graphene structure under different temperatures. A higher temperature can lower the LRS and SET voltage, which indicates that the filament is formed by oxygen vacancies.

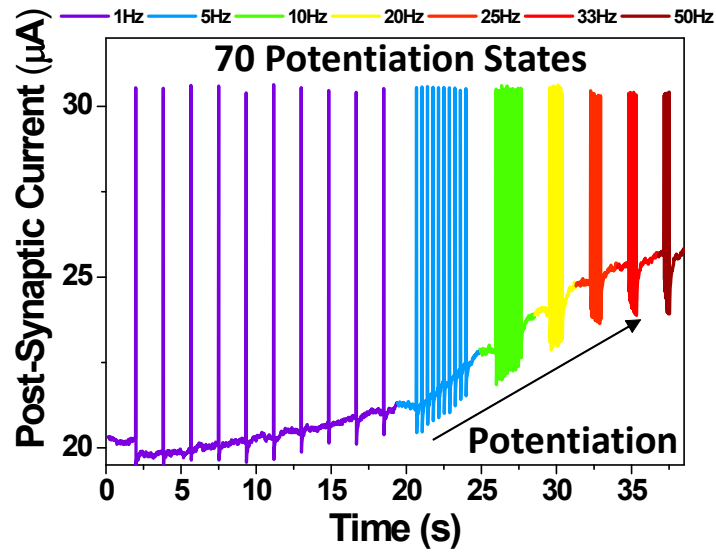


Figure S4. The post-synaptic current (PSC) modulated by 10 ms pulses with different repetition frequency under mode II. The PSC shows 70 potentiation states without saturation. The synaptic strength is related to the frequency of the input pulses, which reproduce the bio-synapse behavior.

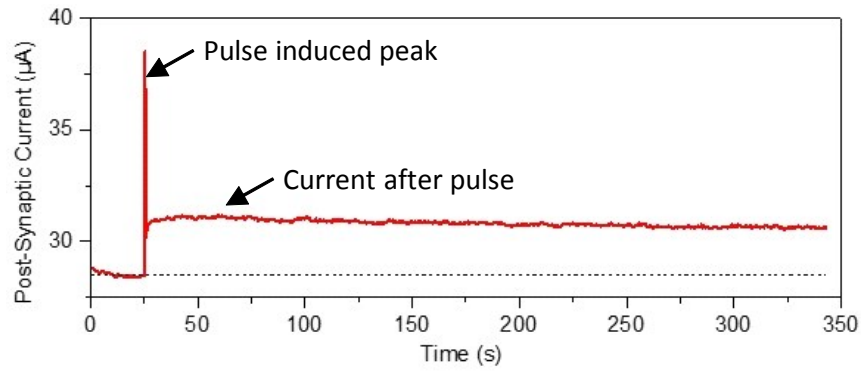


Figure S5. The post-synaptic current after pulse modulation having good retention up to 300 s.

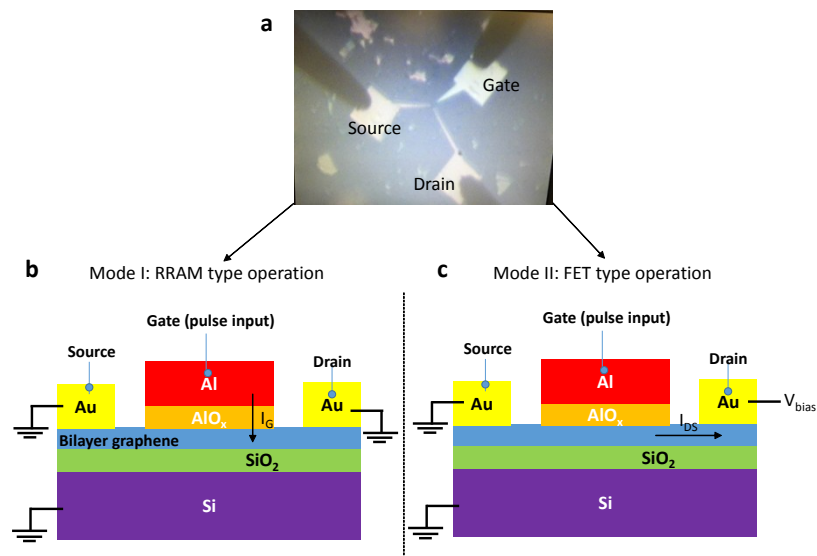


Figure S6. The structure operated in two modes with the same measurement configuration. (a) Measurement setup for one device operated in two modes. (b) RRAM type operation. (c) FET type operation. The main difference is the post-synaptic current definition. In RRAM type operation, the post-synaptic current is defined as gate leakage current (I_G). While in the FET type operation, the post-synaptic current is defined as the drain current (I_{DS}).