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Electronic Supplementary Information for:

Annealing and Polycrystallinity Effects on the Thermal Conductivity of Supported CVD Graphene Monolayers

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Device Fabrication (including details of graphene transfer)

We have employed a suspended electro-thermal micro-bridge device to carry out measurements of thermal transport in Cu-CVD graphene monolayers supported on silicon dioxide (SiO_2). These devices have previously been used to accurately measure the thermal conductivity of monolayer and multilayer graphene exfoliated onto SiO_2.[12,27] However, the reported fabrication scheme, particularly the reactive ion etching of SiO_2 and the wet-etching of underlying silicon to suspend the micro-bridge, resulted in ribbons of hard to remove plasma-hardened residues as well as delamination of graphene from our devices (Figure S1). In addition, we observed an order of magnitude decrease in the temperature coefficient of resistance (TCR) of evaporated Cr/Au (5

nm/45 nm) contacts upon annealing, which significantly affected the sensitivity of our thermal measurements (Figure S2). While Cr/Pt (5 nm/45 nm) resistors did not suffer from such a large drop in TCR upon annealing, the stress in Pt resulted in rapid lift-off that caused tears in graphene near the edges of top side contacts. In order to circumvent these problems, we made two crucial changes to the fabrication process: (1) graphene was transferred using the PMMA-mediated method[41,42] onto partially-fabricated devices, such that SiO_2 etching as well as metallization had already been done; (2) dry-etching of underlying Si was carried out in xenon difluoride instead of in aqueous tetra-methyl ammonium hydroxide (TMAH) or aqueous potassium hydroxide (KOH). This resulted in high yields of measurable devices. The complete details of fabrication are described next.

Our devices were fabricated on heavily Boron doped (1-10 mΩ-cm) 4 in Si <100> wafers with 300 nm wet thermal SiO_2 on top. Alignment marks for electron-beam lithography (EBL), and labels to identify regions of interest were first fabricated by EBL on a 290 nm/70 nm thick 600k/950k PMMA (600k : PMMA-669.04; 950k : PMMA-672.02; ALLRESIST GmbH) double layer. Development in methyl iso-butylketone (MiBK): isopropanol (IPA) (1:2) mixture, descum in an O_2 plasma at 200 W for 20 seconds, was followed by evaporation of Cr/Pt (5 nm/45 nm) and lift off in N-Methyl-2-pyrolidone (NMP) at 80 °C for 1 hour. The wafer was then de-scummed in a O_2 barrel asher at 600 W for 2 minutes.

The SiO_2 layer was subsequently patterned to create micro-bridges using EBL and RIE. The wafer was heated on a hot plate at 180 °C for 5 minutes to dehydrate it, and spun coat with a 290 nm/280 nm PMMA/CSAR double layer (PMMA-669.04; CSAR-6200.09; ALLRESIST GmbH), with the slightly more etch resistant CSAR layer on top. Following EBL, development was carried out in amyl acetate (AR 600-546 developer from ALLRESIST GmbH), the standard

CSAR developer, which also clears the underlying PMMA. The exposed SiO_2 was etched through to the Si below in an RIE using a $CHF_3/CF_4/Ar$ (32:17:2 sccm) plasma (100 W, 30 mtorr) in 20 minutes. About 250 nm of the resist stack remained after RIE. It was partly removed by O_2 RIE (60 W, 200 mtorr, 60s) to get rid of the plasma hardened top and side layers, followed by complete stripping in NMP at 80 °C for 1 hour.

Next, the metal resistances, contacts, and bond pads were fabricated by EBL, metal evaporation (Cr/Pt (2 nm/28 nm)) and lift off using the process identical to the one used to fabricate the alignment marks described above. Separating the two, otherwise identical, steps was a means to achieve better alignment accuracy.

The wafer was then coated with a thick photoresist (AZ4562; MicroChemicals), and immersed in 7% buffered hydrofluoric acid (BHF) for 5 minutes to etch the ~300 nm of SiO_2 on the backside of the wafer. Then, 30 nm of Au was sputtered onto the back side to enable grounding the device during measurements. Finally, the wafer was diced into 15 x 15 mm chips, with horizontal and vertical cuts to half-depth for easy cleaving into four quadrants (7.5 x 7.5 mm) after graphene transfer and patterning (Figure S3a).

The well-known PMMA-mediated method was used to transfer continuous films of Cu-CVD graphene onto our devices.[1–3] The details of our specific transfer process are described below. Monolayer graphene on the growth Cu foil (25 μm thick) was coated with a 120 nm PMMA layer (PMMA 672.03; ALLRESIST GmbH) and baked on a hot plate at 120 °C for two minutes. The coated Gr/Cu was floated face-up on top of an ammonium persulfate (APS; 0.5 M in deionized water) solution in a 30 mL beaker for 10 minutes, and the APS started turning slightly blue in color. The foil was then transferred to a beaker of deionized water (DIW), and the discontinuous graphene film on the backside of the foil detached from it.[4] After rinsing in a

separate beaker of DIW, the Gr/Cu with a backside denuded of graphene was placed in a fresh beaker of APS overnight (~10 hours) to fully etch the Cu foil. The floating PMMA/Gr film was picked up using a clean piece of silicon, and floated on the surface of DIW in a beaker—twice for five minutes each—to rinse off APS, copper and copper sulfate residues that could be so removed.

The chip upon which this film was to be transferred was cleaned in O_2 plasma (600 W, 5 minutes) in a barrel etcher to remove organic residues from the surface. Immediately afterwards, it was immersed in a dilute hydrofluoric acid solution, 48% HF: DIW (1:50) by volume, for 15 seconds to etch away a few nanometers of the exposed SiO_2 surface of the chip. Following this process the surface was hydrophilic, and was used to pick up the cleaned PMMA/Gr film floating on DIW. The chip was then leaned against an inverted watch glass and allowed to dry on the wet bench. After an hour, the water between PMMA/Gr and the device had wicked away and evaporated. The chip was then heated on a hot plate at 60 °C for 5 minutes. Afterwards, the temperature was ramped to 150 °C (above the glass transition temperature of PMMA) over a period of 5 minutes and held there for a further 5 minutes. Following this we observed the shrinking of the height of large wrinkles, and better conformity of the film with the topography of the patterned SiO_2 surface. We then spun a second layer of PMMA on top (290 nm; PMMA-669.04) and baked the chip on a hot plate at 180 °C for 5 minutes. This combined stack of transfer-PMMA and respun-PMMA was used to pattern the transferred film of graphene for thermal measurements (Figure S3a). We found it unnecessary to strip the PMMA used for transfer before proceeding with EBL to pattern the transferred graphene. After EBL and development in 1:2 MiBK: IPA, no large-scale rips or tears were observed in the large areas of exposed graphene (Figure S3b). O_2 RIE (30W, 20 mtorr, 40 s, 45 sccm O2/5 sccm Ar) was used

to etch away the unmasked graphene. The chip is then baked on a hot plate at 150 °C for 5 minutes to reflow the PMMA and improve graphene adhesion to the substrate near the newly created edges (Figure S3c). This step was found vital to largely eliminate peeling of large areas of graphene when PMMA was later stripped in chloroform (or acetone), as shown in Figures S3d and S3e.

The final release of the micro-bridge devices is realized by under-etching Si using XeF_2 gas. The same 570 nm thick PMMA/CSAR double layer resist stack and design, used to etch through SiO_2 to the Si below, was used to mask all areas of the device except the previously exposed Si surface (Figure S3f). This prevented the fluorination of graphene by exposure to XeF_2.[5] The isotropic etching of Si was carried out in a commercially available SPTS Xactix X4 etching system. The release of the micro-bridges was complete after 4 pulses, 8 seconds each, in a XeF_2/N_2 (3:10 Torr) gas mixture (Figure S3g). The pulsed etching was used to prevent over-heating of the resist mask in suspended areas of the device due to the heat released during the exothermal chemical reaction between XeF_2 and Si. To strip the resist mask, we first etched the heavily fluorinated outer layers in a lower power isotropic O_2 RIE process (60W, 200 mTorr, 40s). This vital step was necessary to achieve the levels of resist residue seen in graphene devices that weren't exposed to XeF_2. If skipped it resulted in the collapse of a presumably fluorinated film of residue onto the surface of graphene, which could not be removed by solvents typically used for stripping resist (Figure S4a). Even annealing at 300 °C for 2 h in Ar/H2 (100 sccm/900 sccm) was ineffective (Figure S4b). While annealing in Ar/O_2 (375 sccm/125 sccm) at 300 °C for 2 h was effective, it could cause damage due to the combination of a reactive gas (oxygen) and the heightened reactivity of graphene supported on SiO_2 (Figure S4c). The chips were then immersed in acetone for 3 hours, transferred to chloroform and left overnight. Next,

the solvent was replaced with IPA by successive transfers into beakers containing IPA and dried using critical point drying to prevent sticking of the suspended micro-bridges to the bottom of the etch pit during evaporative drying (Figures S3h and S3i).

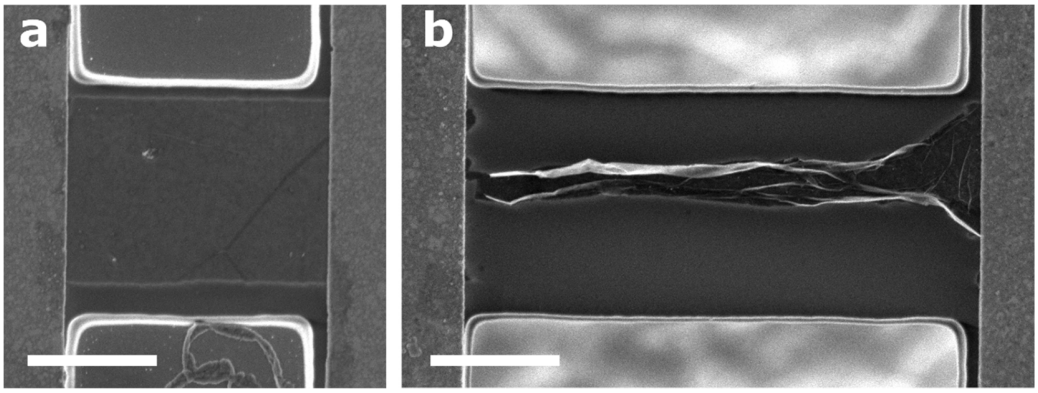

Figure S1. (a) SEM image of an ~1.4 μm wide strip clamped with evaporated Cr/Au contacts, shown here after the supporting SiO_2 layer was patterned by reactive ion etching. Plasma-hardened ribbon of resist residue can be seen adhering to the lower edge of the SiO_2 bridge. (b) After the underlying Si was etched in hot aqueous tetra-methyl ammonium hydroxide (TMAH) and the samples were dried by critical point drying, the graphene strips were found torn after rolling up due to loss of adhesion with the SiO_2 substrate. The strip shown here is 4 μm long. Such loss of adhesion resulted irrespective of whether the graphene was coated with resist during the TMAH etching. This loss of adhesion did not occur when Si was etched using XeF_2 gas instead. Both scale bars are 1 μm.

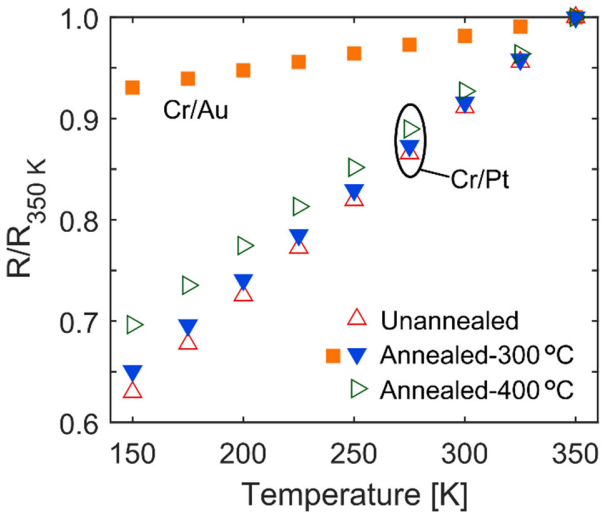

Figure S2. Electrical resistance (R) versus temperature (T), normalized by the value of R at 350 K, of nominally identical resistance-thermometers from different devices. The greater the slope of $R(T)$, the higher is the temperature coefficient of resistance (TCR), and the more sensitive the resistance-thermometer is. While 5 nm Cr/45 nm Pt only shows an ~19% decrease in TCR after annealing at 400 °C in Ar/H_2 for 2 hours, 5 nm Cr/45nm Au shows an ~81% decrease in TCR. This results in a two-fold increase in uncertainty of a typical thermal conductance measurement carried out in this study.

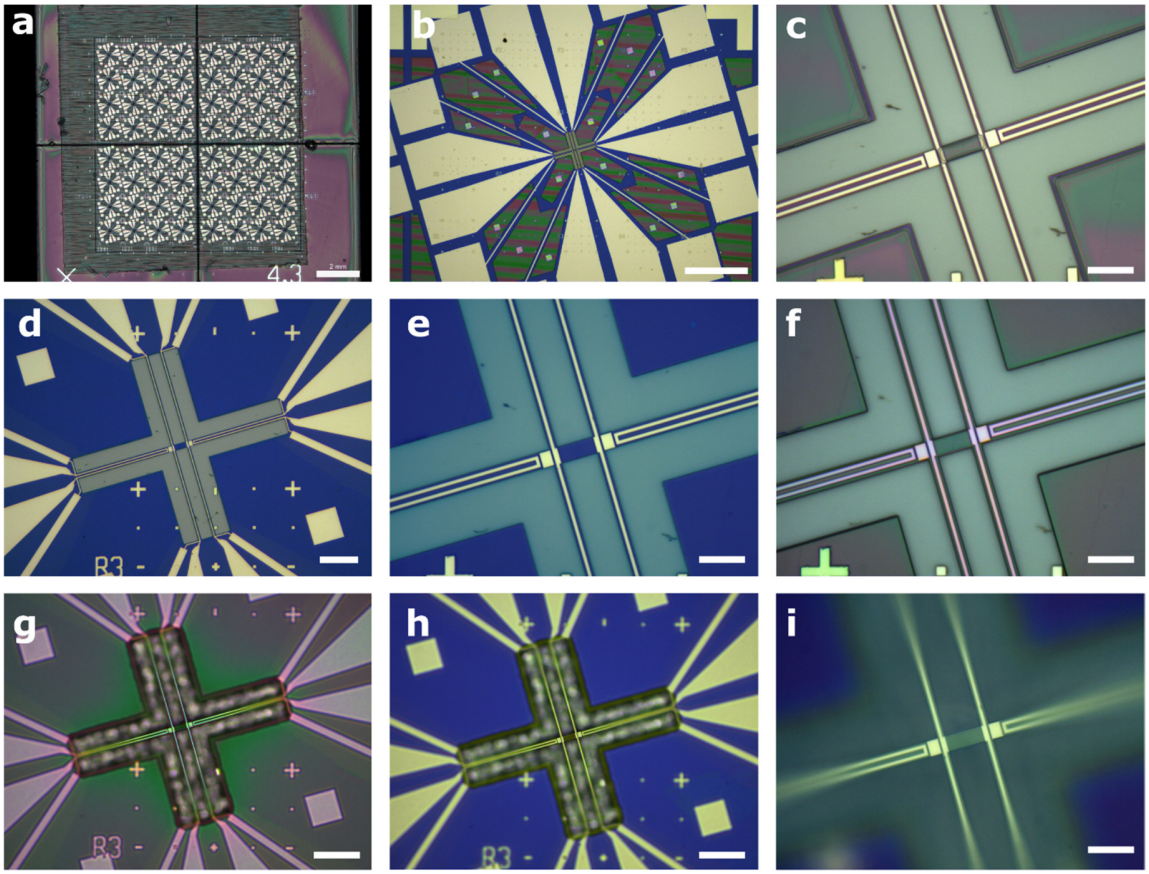

Figure S3. Micrographs during various stages of fabrication of suspended micro-bridges integrated with graphene strips. (a) Chip with 64 pre-fabricated devices, pre-diced into four quadrants, after PMMA assisted transfer of CVD graphene, drying and spin-coating of second PMMA layer. (b) Magnified view of one device after EBL and PMMA development. (c) Central device area after etching of exposed graphene and baking, to reflow PMMA and to improve graphene adhesion at edges. (d) After stripping resist, the difference in contrast between areas with and without graphene adjacent to the central cross structure becomes evident. (e) Magnified view of the same device where a wrinkle can be seen in the central graphene. (f) After patterning resist to protect graphene and device during XeF2 exposure. (g) Device has been suspended by under-etching Si in XeF2. (h),(i) Fabrication is complete after stripping resist and critical point drying. The suspended bridge bows upwards due to intrinsic stress in SiO2. Scale bars for parts a–i are 2 mm, 200 µm, 10 µm, 25 µm, 10 µm, 10 µm, 25 µm, 25 µm and 10 µm respectively.

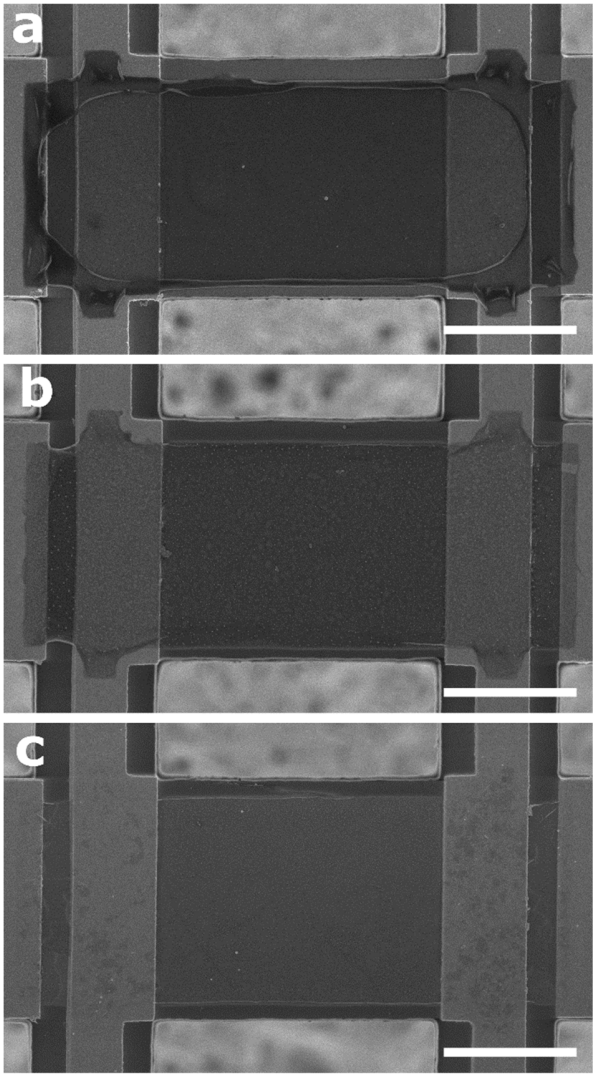

Figure S4. (a) SEM image of a suspended micro-bridge with graphene integrated, showing a collapsed layer of fluorinated polymer entirely covering the surface of graphene. The oval fold is clear evidence for the origin of this encapsulating layer. It was formed on the surface of the ~600 nm thick resist mask by its reaction with XeF_2, creating a solvent stable scaffold which collapsed onto graphene when the underlying, un-fluorinated resist was dissolved in chloroform. (b) Annealing at 300 °C in Ar/H_2 at atmospheric pressure for 2 hours, only resulted in partial removal of this layer. Obvious roughness is observed on the graphene surface. (c) Annealing at 300 °C in Ar/O_2 at atmospheric pressure for 2 hours was much more effective for removing this layer. However, it was desirable to find a method of removing the fluorinated polymer layer before it adhered to graphene. All scale bars are 2 μm. Acceleration voltage was 1 kV for all.

Visualizing the Polycrystallinity of Graphene

Annealing graphene films on copper at 150 °C under a N_2/O_2 (375 sccm, 125 sccm) atmosphere oxidized the copper underneath grain boundaries. While large grain graphene films could be annealed for significantly longer periods of time, the copper underneath small grain graphene oxidized very quickly, requiring careful optimization of the annealing time to retain the utility of the technique. This technique was used to identify that graphene of type G1 has grains several microns in size, while graphene of type G2 had an average grain size of ~200 nm, as shown in Figure S5.

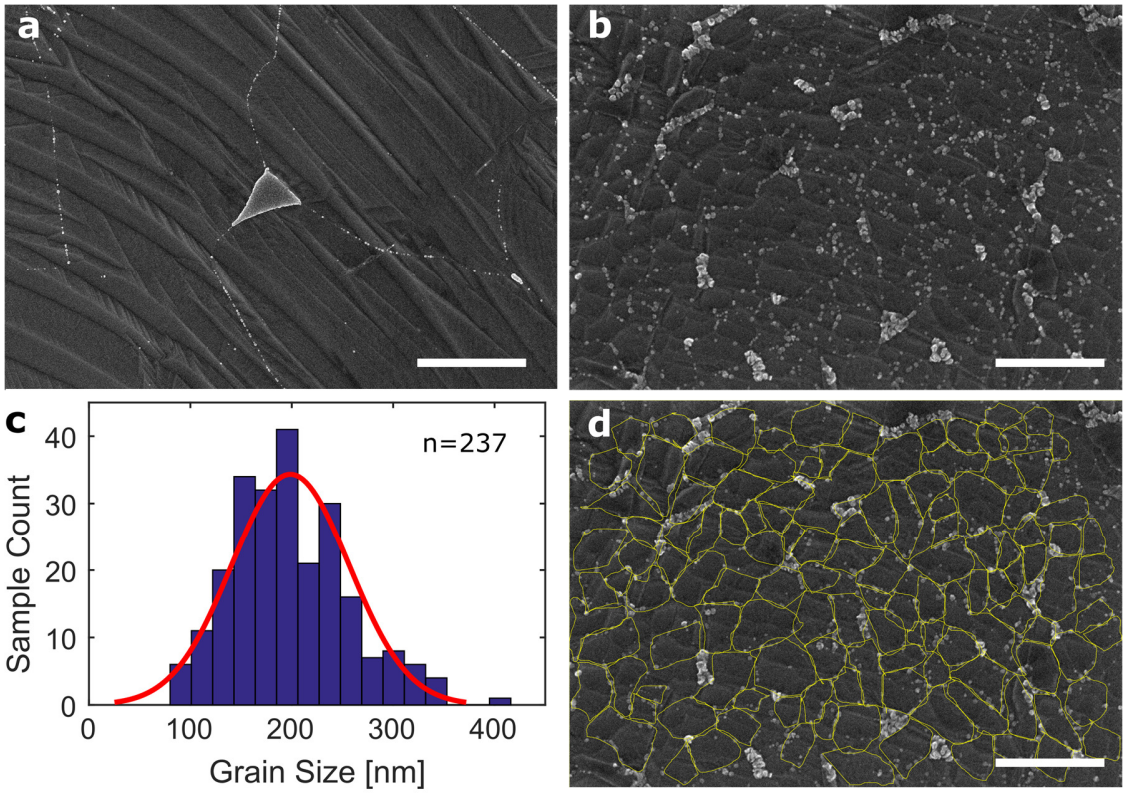

Figure S5. Grain boundaries of (a) large grain (G1) and (b) small grain (G2) graphene revealed by annealing grown graphene films on copper in N_2/O_2 at 150 °C for 5 minutes. We used films with almost, but not complete graphene coverage to help identify edges to enable image-

processing to determine grain sizes. (c) Histogram of grain size of G2 obtained from two images including part b, by manual segmentation as shown in (d). Scale bars for parts a,b and d are 1 μm, 500 nm and 500 nm respectively.

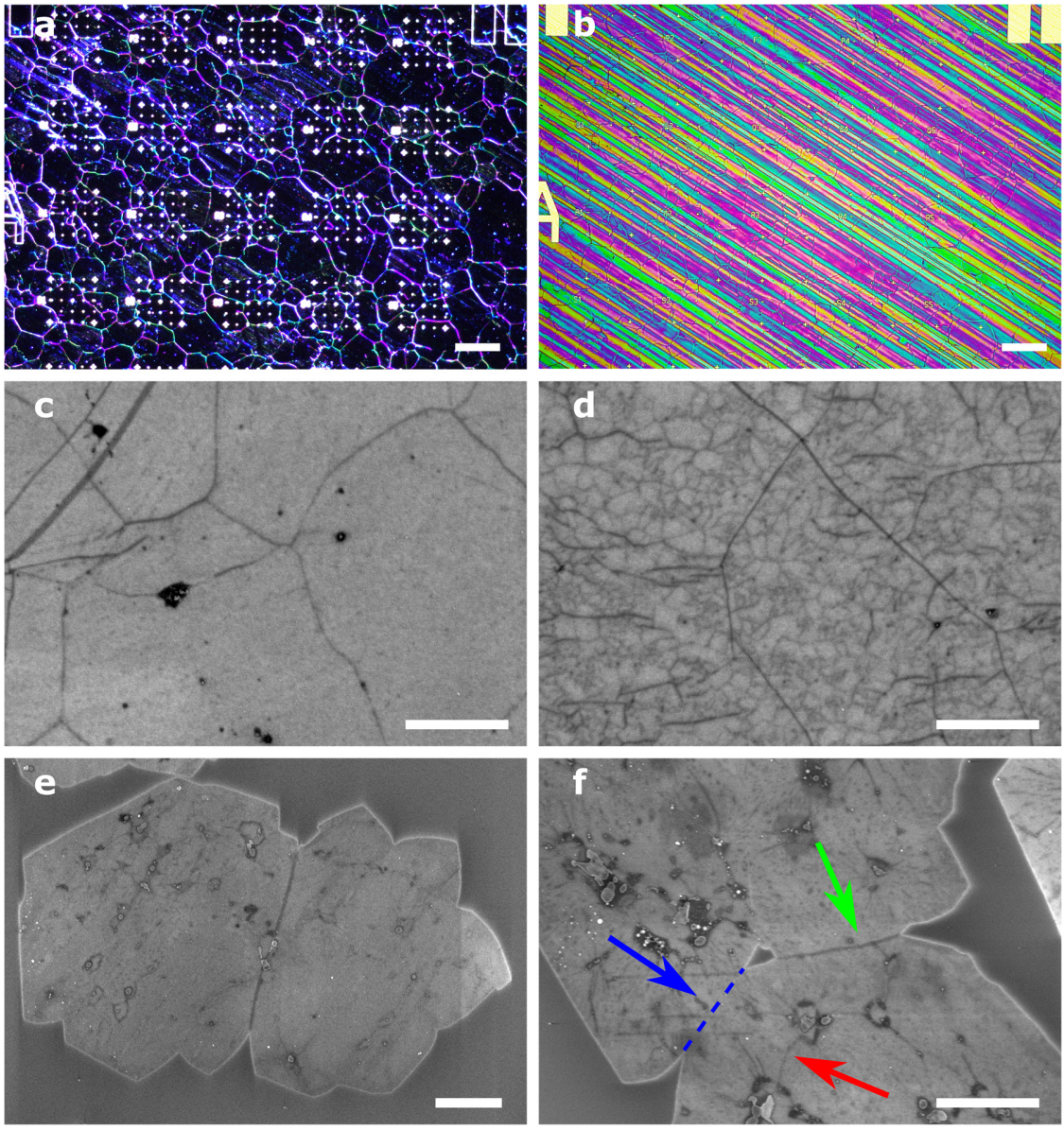

Figure S6. (a) Dark field microscopy of PMMA on graphene after transfer shows large scale wrinkles form areas typically several tens to hundreds of microns in size. (b) Bright field optical microscopy reveals the macroscale effect on PMMA thickness (which produces the color contrast) of parallel striations observed on copper foils used for graphene growth. These stripes are not observed on graphene in our study after PMMA is removed. What remains on graphene after transfer, PMMA removal and annealing are large scale wrinkles, and other smaller scale features which can be correlated to the level of polycrystallinity of graphene, as seen in the SEM images of (c) large and (d) small grain graphene on silicon dioxide. (e) The contrast observable by SEM imaging at the junction between two large grains after transfer and annealing is clearly illustrated here. (f) However this observation is not an unambiguous signature of a grain boundary, since the lines of dark contrast do not appear at all grain boundaries—it can be seen at the boundary marked with a green arrow, but not at the one with a blue arrow. Moreover, we observe these lines of dark contrast also in the interior of individual grains (red arrow). Therefore while this feature is a useful indicator, its quantitative utility is limited. Scale bar for parts a,b is 100 μm, and for parts c–f is 1 μm.

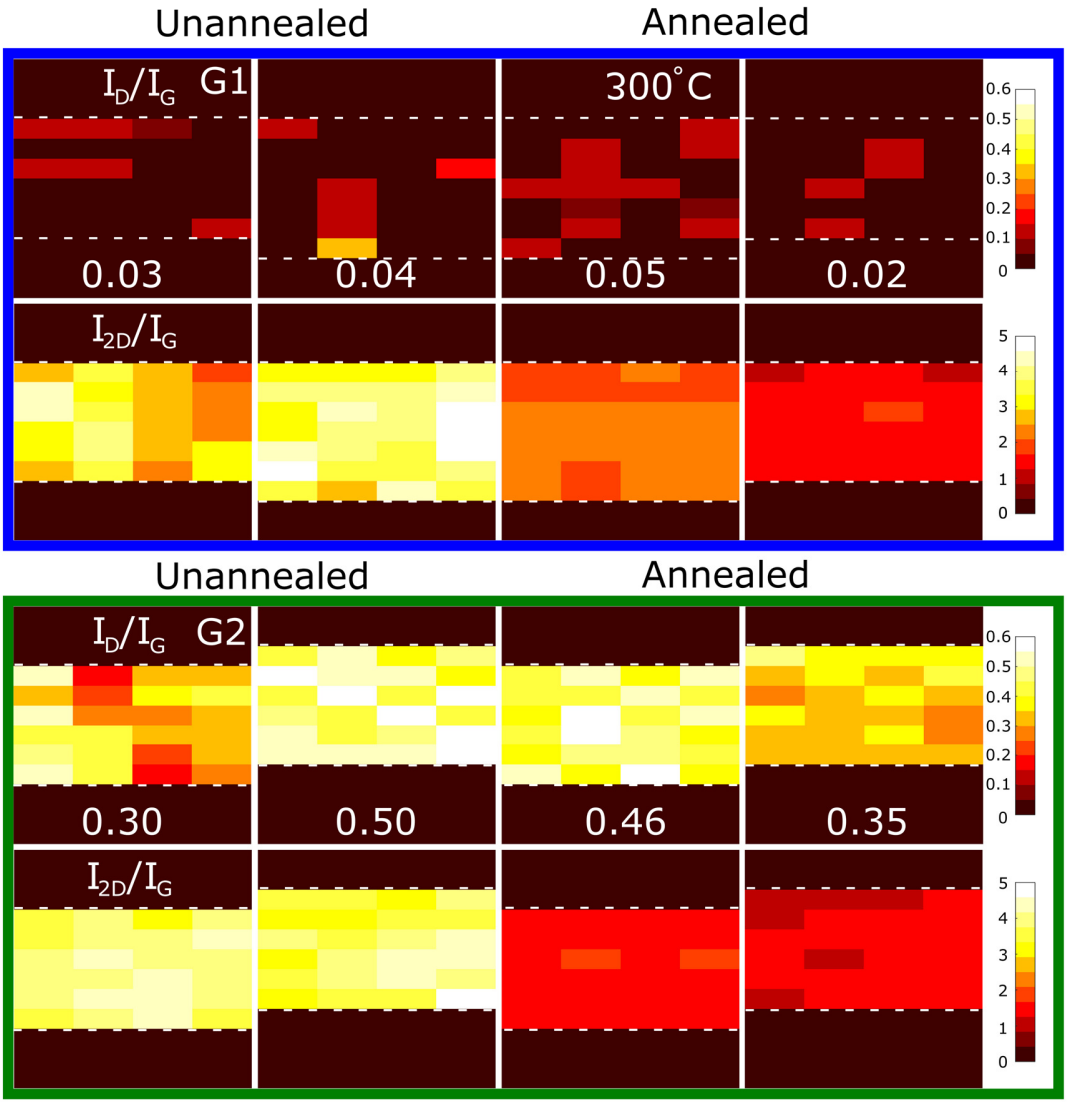

Figure S7. Raman maps of I_D/I_G and I_{2D}/I_G of every graphene strip on a micro-bridge whose thermal conductance measurement is reported in this study. The maps for samples of type G1 are in the top two rows (within the blue rectangle), and those of G2 are in the bottom two rows (within the green rectangle). For each sample, the I_D/I_G map is directly above the I_{2D}/I_G map. The average I_D/I_G value is displayed in the bottom of each map. Unannealed samples are in the first two columns, and annealed samples are in the last two columns. One sample was annealed at 300 °C, mentioned in the corresponding Raman map; all other samples were annealed at 400 °C.

Some maps are one pixel wider than others because of imperfect alignment between the stepping of the Raman mapping grid with the edge of the graphene sample.

Device Packaging and Measurement Scheme

Some details of device packaging and the measurement setup are identical to those we recently reported and are only repeated here for convenience.[6] One chip quadrant (7.5 x 7.5 mm) consisting of 16 micro-bridge devices was fixed to a 24 pin ceramic dual inline package (DIP; SB2438001; Global Chip Materials) using high vacuum thermal grease (Krytox LVP grease; DuPont). The use of thermal grease rather than conductive silver paint facilitated easy removal of chips from the package after measurement for further characterization. Wire bonds were made to the contact pads of the device to be measured, using an ultrasonic wedge bonder. The DIP was mounted in a shorted socket and grounded through a 10 MΩ ballast resistance to the same point as the bonding probe. The wire-bonded packages were mounted to the socket on the cold finger of a continuous flow cryostat (ST-100; Janis) using Krytox LVP grease to ensure good thermal contact between the package and the cold finger. An inner radiation shield made of brass mounted to the cold finger and an outer radiation shield of aluminum were used to minimize radiative heat loss. The measurements were also performed in high vacuum ($< 10^{-5}$ mbar) to prevent convective heat loss from the device. The sample temperature is measured using a diode thermometer mounted on the cold finger and regulated using PID control of the heating power of a button heater mounted on the cold finger, while maintaining a constant flow of liquid nitrogen. Temperature stability of ±30 mK was achievable. We performed measurements for sample temperatures from 150 K up to 350 K. We started at the lowest temperature and measured

upwards. After each temperature is set, we waited for it to stabilize to better than ±30mK over a period of a minute, then waited 5 minutes to allow the sample to equilibrate with the cold finger and then started the measurements at that temperature.

To determine the thermal conductance of graphene supported on SiO_2 (G_s), we first measured the total thermal conductance of graphene and SiO_2 (G_{tot}) and then subtracted the thermal conductance of SiO_2 alone (G_{bl}), measured from a nominally identical device fabricated without graphene. The measurement scheme used in our study follows the work of Seol et al.[7] To measure the thermal conductance of a sample bridging the two sides of the micro-bridge, the resistance of the four resistance thermometers—R1, R2, R3 and R4—were precisely measured, as different levels of heat was dissipated in R1 by a DC heating current (I_h) passing through it. All four resistances were measured using a four-probe scheme to eliminate contact and lead resistances. R1 was sourced and measured by the same DC instrument (Keithley 2636A). At each temperature set point a forward and reverse dual sweep of DC heating currents in the 20-80 μA range was performed, starting with the positive currents in ascending order up to the maximum, then in descending order down to the largest negative current, and finally back up to zero. This enabled us to account for DC offsets in voltage measurement during post-processing. R2, R3 and R4 were measured using two lock-in amplifiers (SR850; Stanford Research Systems). R2 and R3 were measured by one lock-in amplifier (983 Hz) in two separate measurement runs, while R4 was measured by the other lock-in (971 Hz) in both runs. A 500 nA AC excitation current for lock-in measurement of voltage across a resistance, was generated by passing a 5 V_{rms} voltage generated by the respective lock-in amplifier through a high precision 10 MΩ resistor (Caddock USF370).[8] Lock-in offset and expand (50-100x) functions were used

to improve the resolution of lock-in voltage measurement, since changes in voltage during a typical sweep of heating currents was far below the full scale voltage.[9]

Uncertainty Analysis

The resistance (R_{ac}) of three of the four resistance thermometers (R2,R3 and R4) are measured using an AC current generated by passing an output voltage (V_{out} = 5 V_{rms}) from the lock-in amplifier through a 10 MΩ precision resistance (5 ppm/°C).[8] The stability of V_{out} is 50 ppm/°C. The uncertainties in both these quantities are calculated using 0.5 °C as the room temperature variation during the experiment. The uncertainty in voltage (V_{ac}) measured by the lock-in, is calculated as the standard deviation of 640 samples collected over 10 s for each heating current (I_{dc}) set point.

$$\frac{\delta R_{\mathrm{ac}}}{R_{\mathrm{ac}}} = \sqrt{\left(\frac{\delta V_{\mathrm{out}}}{V_{\mathrm{out}}}\right)^2 + \left(\frac{\delta R_{10\mathrm{M}\Omega}}{R_{10\mathrm{M}\Omega}}\right)^2 + \left(\frac{\delta V_{\mathrm{ac}}}{V_{\mathrm{ac}}}\right)^2} \tag{S1}$$

The U-shaped resistance through which the DC heating current (I_{dc}) is passed, R1, is measured using a DC voltmeter. The uncertainties in current and voltage are again calculated as the standard deviation of 100 samples collected over 10 s for each current set point.

$$\frac{\delta R_{\mathrm{dc}}}{R_{\mathrm{dc}}} = \sqrt{\left(\frac{\delta I_{\mathrm{dc}}}{I_{\mathrm{dc}}}\right)^2 + \left(\frac{\delta V_{\mathrm{dc}}}{V_{\mathrm{dc}}}\right)^2} \tag{S2}$$

The resistance of a resistance thermometer in the limit of zero dissipated power in R1, at a particular environment temperature (T_i), is taken as the intercept of a line fit to each resistance as a function of the dissipated power. Since the process is identical for all four resistances, we simply refer to this as R_0, without using indices to distinguish between the four resistances. The

uncertainty in R_0 is computed from the linear regression itself, using the *polyconf* function in MATLAB.

The increase in resistance in response to a certain heating current, ΔR_j is converted to a temperature excursion, ΔT_j, by calculating the rate at which R_0 changes with the environment temperature, T_i. for that particular resistance. The inverse of this rate, m, relates the resistance and temperature excursions, as, $\Delta T_j = m\Delta R_j$. We calculate m as a forward two-point slope, i.e. at environment temperatures T_i and T_{i+1}. The uncertainty, δT, in T_i and T_{i+1}, is 50 mK. Note that j is the index used to denote measurements collected at different levels of dissipated power in R1 at the same environment temperature.

$$m = \frac{T_{i+1} - T_i}{R_0(T_{i+1}) - R_0(T_i)} \tag{S3}$$

$$\frac{\delta m}{m} = \sqrt{2\left(\frac{\delta T}{T_{i+1} - T_i}\right)^2 + \left(\frac{\sqrt{\delta R_0(T_{i+1})^2 + \delta R_0(T_i)^2}}{R_0(T_{i+1}) - R_0(T_i)}\right)^2} \tag{S4}$$

$$\frac{\delta \Delta R_j}{\Delta R_j} = \frac{\delta R_j + \delta R_0}{R_j - R_0} \tag{S5}$$

$$\frac{\delta \Delta T_j}{\Delta T_j} = \frac{\delta m}{m} + \frac{\delta \Delta R_j}{\Delta R_j} \tag{S6}$$

Following the method used by Seol et al.,[7] the temperature excursions of all four resistances can be used to calculate the beam and sample thermal resistances, R_b and R_s, respectively. By sample we refer to the combined thermal resistance of graphene and SiO_2 bridging the two sides of the device, or SiO_2 only—in a blank device. For brevity, we drop the Δ while referring to temperature excursions, as well as the j index, in the following discussion.

$$\frac{\delta R_b}{R_b} = \frac{\delta P}{P} + \frac{\sqrt{\delta T_1^2 + \delta T_2^2 + \delta T_3^2 + \delta T_4^2}}{T_1 + T_2 + T_3 + T_4} \tag{S7}$$

$$\frac{\delta R_{\mathrm{s}}}{R_{\mathrm{s}}} = \frac{\delta R_{\mathrm{b}}}{R_{\mathrm{b}}} + \frac{\sqrt{\delta T_2^2 + \delta T_3^2}}{T_2 - T_3} + \frac{\sqrt{\delta T_3^2 + \delta T_4^2}}{T_3 + T_4} \tag{S8}$$

R_s at a particular environment temperature is then determined as the weighted average of R_s at different P, with the weights determined by the uncertainties.[10] The inverse of R_s is the sample conductance, which is G_{tot} or G_{bl}, as the case maybe. The thermal conductance of graphene, G_{Gr}, is calculated as the difference between G_{tot} and G_{bl}. Therefore,

$$\delta G_{\mathrm{Gr}} = \sqrt{\delta G_{\mathrm{tot}}^2 + \delta G_{\mathrm{bl}}^2} \tag{S9}$$

Finally, using the length (L) and width (w) of the graphene strip between the metal contacts, measured by SEM, the thermal conductivity of graphene is calculated. The uncertainties in length and width are 100 nm and 50 nm respectively, with L~8.1–8.3 μm and w~2.9–3.1 μm, depending on the device.

$$\frac{\delta \kappa}{\kappa} = \sqrt{\left(\frac{\delta G_{\mathrm{Gr}}}{G_{\mathrm{Gr}}}\right)^2 + \left(\frac{\delta L}{L}\right)^2 + \left(\frac{\delta w}{w}\right)^2} \tag{S10}$$

Finite Element Modeling to Compute Systematic Errors in Measurement due to Contact and Internal Thermal Resistances

3D finite element computations using COMSOL Multiphysics software (version 5.2) were performed to determine the effect of thermal contact resistance on the measured thermal conductances in our experiments. The simulations were performed on a geometry nearly identical to the devices used in our experiments. The minor difference will be discussed subsequently. Three-dimensional steady state heat conduction model was solved in the simulation domain using an iterative solver. Only the suspended area of the device was used in the simulation, and the temperature was set to that of the ambient at the ends of all beams. Insulating boundary conditions were used on all other external surfaces. Radiative heat transfer was not considered because it was estimated to be insignificant compared to typical dissipated power O(10) μW and average temperature excursions of less than 20 K in all our experiments. Interfaces between different materials were modeled using the built-in "Thin Layer" node, where interfacial thermal resistances could be specified. The physical thickness of graphene was increased to 3.4 nm to facilitate meshing,[7] and its thermal conductivity (κ_{Gr}) was set to one-tenth the desired value to achieve the same theoretical thermal conductance.

The interfacial thermal resistance (R_{int}) between exfoliated graphene and SiO_2 has been measured using the 3ω method to be in the range 0.5–1.2×10^{-8} m^2K/W in the temperature range of 150 to 310 K.[11] In each of the four samples measured in that work, R_{int} remains nearly constant in this temperature range, and weakly increases thereafter, down to 42 K. The graphene flakes had been annealed at 400 °C before 30 nm of SiO_2 was evaporated on top, to produce a sandwich structure with two graphene-SiO_2 interfaces in series. Due to the good adhesion

between CVD graphene and SiO_2 in our devices, after the transfer and post-baking processes, R_{int} with SiO_2 for an unannealed sample is expected to be of the same order of magnitude.

The value R_{int}~2–5×10^{-8} m^2K/W in a one-dimensional axisymmetric thermal conduction model with heat loss to the substrate, was found to fit Raman optothermal data obtained on unannealed CVD graphene transferred onto an Au surface.[12] This value is comparable to R_{int} ~ 4×10^{-8} m^2K/W, measured using time domain thermoreflectance (TDTR) for an Au layer evaporated on top of graphene on SiO_2,[13] indicating that with regards to thermal transport, the two types of interfaces—namely, metal evaporated on top of graphene and graphene transferred onto a clean metal surface—are similar. It is therefore reasonable to assume that R_{int} for unannealed CVD graphene to Pt in our devices is comparable to these values.

Another interface of significance in our devices is this between the Cr/Pt resistance and the SiO_2 substrate. It is however a clean interface, because of the use of oxygen plasma descum before metal evaporation, carried out at a pressure lower than 5×10^{-7} mbar. At room temperature, R_{int} of 0.7×10^{-8} and 0.5×10^{-8} m^2K/W for interfaces of Si with Cr and Pt, respectively, have been measured using TDTR.[14] The comparable Debye temperatures of Si (650 K) and SiO_2 (550 K) lead to the expectation of a comparable R_{int} between Cr/Pt and SiO_2 as with Si. In fact, R_{int} for Ti/Au with SiO_2 at room temperature is about 1×10^{-8} m^2K/W,[15] and considering that Ti and Au have significantly lower Debye temperatures than Cr and Pt respectively,[14] leading to a greater mismatch with the SiO_2 substrate, R_{int} is expected not to exceed this value at room temperature in our devices. Moreover, calculations using the diffuse mismatch model also showed that R_{int} remains nearly constant from room temperature down to 100 K.

Thermal conductance in our simulations is calculated analogously to our experiments, by computing the average temperature of all the resistance thermometers for a set level of power

dissipated by uniform volumetric heating in one of the U-shaped resistors, and using the analytically derived formulae relating sample and beam thermal resistances to these temperatures. Thermal conductance of supported graphene is then calculated by subtracting the computed thermal conductance of a blank device.

We made a necessary change to the geometry of the device in the simulation, which is different from that of the device used in experiments. While in the actual device the top surface of the metal is above the plane of SiO_2 by the thickness of the evaporated layer, in the simulation we raise the level of SiO_2 in the central bridge, such that it is level with the surface of the metal contacts on either side. This facilitates modeling graphene as a planar rectangular sheet with a small thickness, obviating the need to address the step at the edge of the metal contact area. Before using this modified geometry, we determined the combination of values for thermal conductivity of SiO_2 (κ_{SiO2}) and the metal lines (κ_M) that would best fit the measured values of beam and blank bridge thermal conductance, and found the values of 1.244 W/mK for κ_{SiO2} and 37.0 W/mK for κ_M to be appropriate. R_{int} between the metal lines and SiO_2 ($R_{M\text{-}SiO2}$) was set to 1×10^{-8} m^2K/W in these simulations. We find that the thermal conductance of the device varies by less than the random uncertainties in a typical thermal conductance measurement in experiments, when $R_{M\text{-}SiO2}$ is doubled from 1 to 2×10^{-8} m^2K/W. Based on this we set $R_{M\text{-}SiO2}$ to 1×10^{-8} m^2K/W in subsequent simulations.

Next, using the thermal conductivities for metal and SiO_2 stated above in the modified geometry, and setting R_{int} between graphene and the metal ($R_{Gr\text{-}M}$) at the contact area to be 1×10^{-7} m^2K/W, we varied R_{int} between graphene and SiO_2 ($R_{Gr\text{-}SiO2}$) from 1×10^{-6} m^2K/W to 1×10^{-8} m^2K/W, and found the relative difference in thermal conductance of graphene between the two extremes to be less than 1 %. Varying $R_{Gr\text{-}M}$ between 1×10^{-6} m^2K/W to 1×10^{-8} m^2K/W keeping

$R_{Gr\text{-}SiO2}$ equal to 1×10^{-7} m^2K/W results in a 2.7 % relative difference between the two extreme values, lower than random uncertainty in graphene thermal conductance from our experiments.

We find that within the stated reasonable limits for different R_{int}, the measured thermal conductance of graphene from simulations is lower than the theoretically expected thermal conductance by ~11–13 %. These trends remain similar when the set thermal conductivity of graphene (κ_{Gr}) is decreased from 38.6 W/mK (representative scaled value for unannealed G1 at 300 K) to 10.8 W/mK (representative scaled value for annealed G2 at 300 K). The systematic under-estimation of graphene thermal conductance in this case is slightly less, ~9–11 % for the same range of R_{int} values. Therefore, thermal contact resistance is not the cause for the reduction in κ observed after annealing, because, if anything, the systematic error is less when κ of graphene is smaller.

The same analysis was also done on the results of simulations performed using 0.895 W/mK for κ_{SiO2} and 26.5 W/mK for κ_M, which were values found to fit measurements of a blank device at 150 K. Using the maximum and minimum values of κ_{Gr} measured at 150 K, ~20 W/mK and 5 W/mK, showed that the systematic under-estimation is ~11–12 % and ~10–11 % for higher and lower κ_{Gr} respectively, comparable to the values at 300 K.

Due to the small variation of the percentage of systematic error for the entire temperature range, we keep the correction factor constant at all temperatures for a particular sample. We also use the same correction factor for all samples of a certain type, due to the similarity in the measured thermal conductance for such samples. For G1 samples, the systematic error is taken as 12% and 11% for unannealed, and annealed samples, respectively. For G2 samples, the systematic error is taken as 11%, 10%, 10% and 11%, for unannealed, annealed, fluorinated and encased samples, respectively.

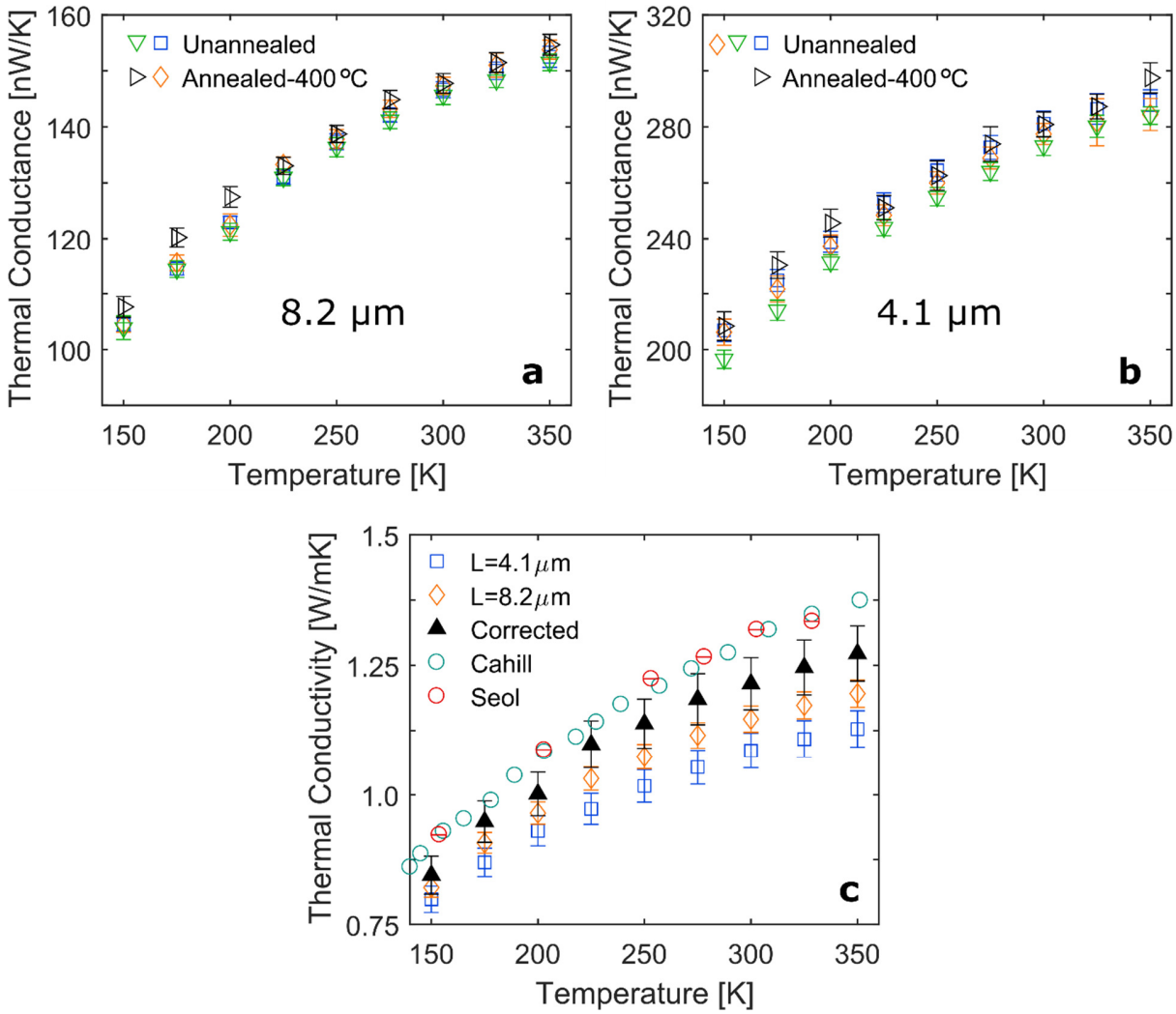

Figure S8. Thermal conductance versus temperature measurements of four blank devices of lengths (a) 8.2±0.1 μm and (b) 4.1±0.1 μm each. The width is 3.5±0.05 μm, and SiO_2 thickness is 300±3 nm for all devices. As expected, annealing at 400 °C for 2 h in Ar/H_2 at atmospheric pressure, did not affect the thermal conductance of blank devices. These measurements were averaged to calculate the background thermal conductance (G_{bl}) for devices of a certain length. (c) Due to the finite internal resistance of the micro-bridge devices, thermal conductivity of SiO_2 calculated using G_{bl} and the bridge dimensions, result in values under-estimated by ~6% and ~11% for the longer (diamonds) and shorter (squares) devices, respectively, from the value obtained after correcting for the offset resistance (triangles). Also shown are values for thermal conductivity of bulk a-SiO_2 measured using the 3ω method,[16] and 300 nm thick thermal SiO_2 measured with a thermal bridge similar to this study[7].

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