Electronic Supplementary Material (ESI) for Nanoscale.
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Supplementary Information

FIGURE CAPTIONS

Figure S1 | Device Fabrication Process (I) The fabrication started with a silicon on insulator (SOI) (Si (1µm) / SiO_2 (2µm) /Si stack) wafer substrate. A thin layer of plasma enhanced chemical vapour deposition (PECVD) silicon dioxide (200nm thick) was deposited on the SOI wafer substrate; **(II)** Self-powered parallel electron lithography (SPEL) was used to pattern the e-beam resist, and the pattern was transferred to SiO_2 using SiO_2 reactive ion etching (RIE), using e-beam resist as the etching mask; **(III)** The silicon NW pillar arrays were formed using silicon RIE with patterned SiO_2 nano-posts as the etching mask; **(IV)** A thick layer of PECVD SiO_2 was deposited on the back side of the SOI wafer; **(V)** Optical lithography was used to pattern the backside circular cavity using backside alignment, and followed by SiO_2 RIE. The SOI wafer Si substrate was etched through by Si deep RIE using the backside PECVD SiO_2 layer as the etching mask and the SOI buried SiO_2 layer as the stopping layer.

Figure S2 |Effect of damping on the force bifurcation diagram Simulations for the effects of linear, nonlinear and combinational damping on the force bifurcation diagram using Eq. 4 with β, ω, ω_0 set to unity **(a)** purely linear damping with $\alpha = 0.5$, $\gamma = 0$; **(b)** purely nonlinear damping with $\alpha = 0$, $\gamma = 0.5$; **(c)** combinational damping with $\alpha = 0.5$, $\gamma = 0.5$

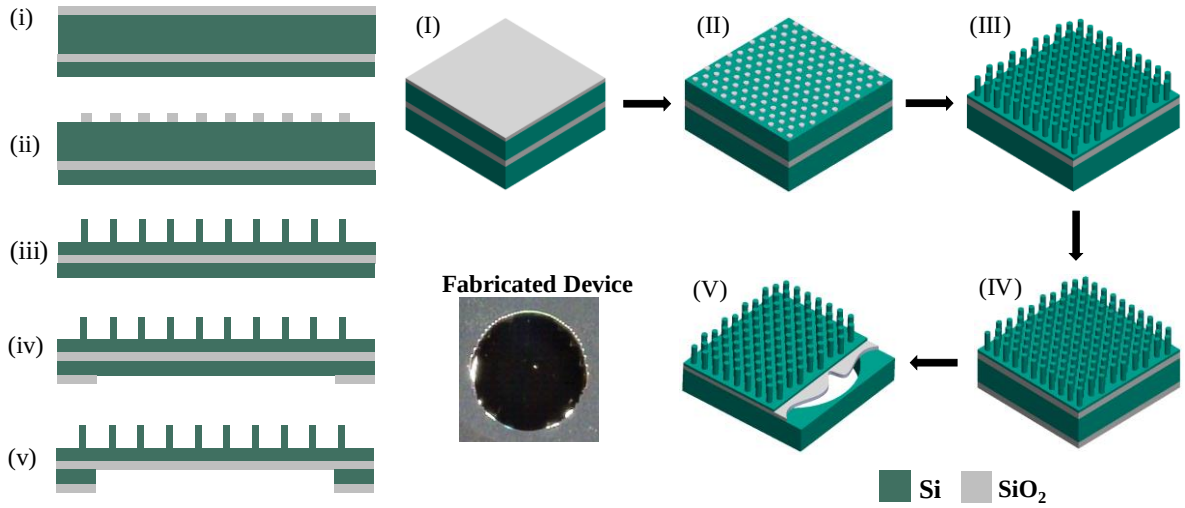
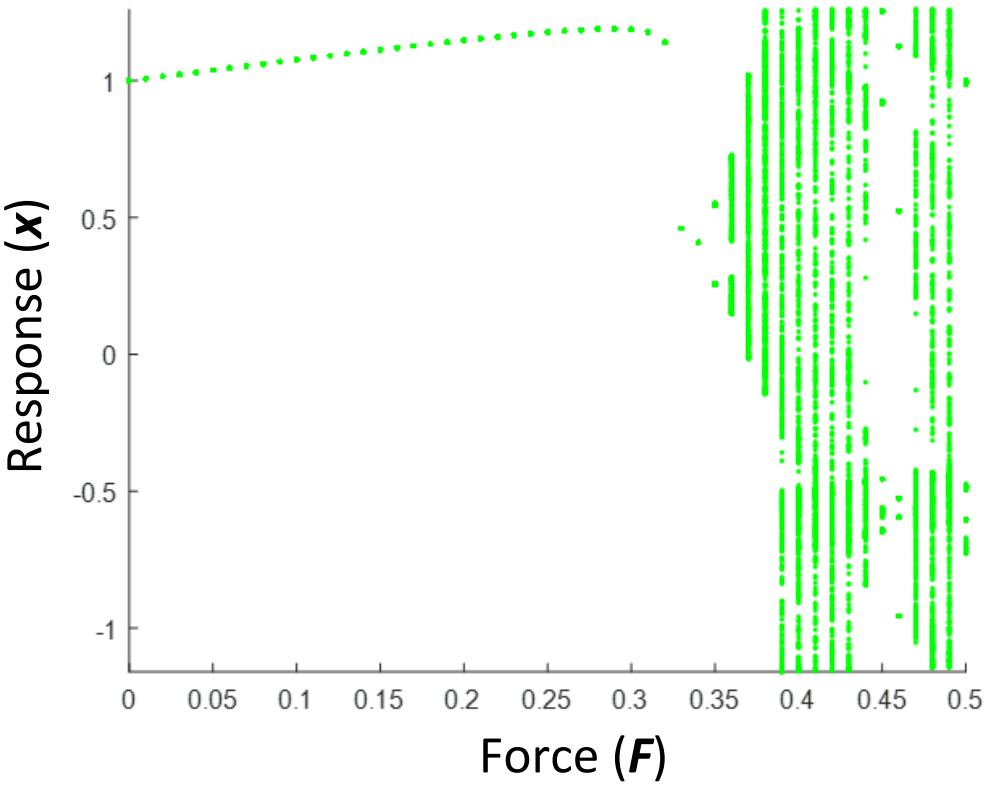
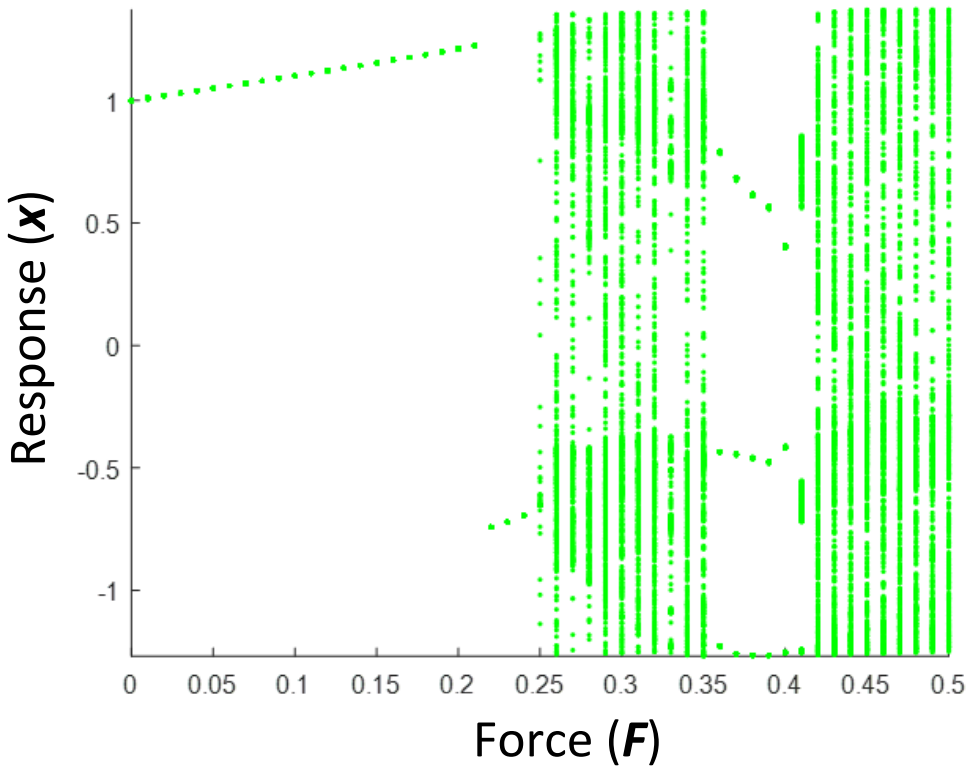


Figure S1

(a)


Response (x)
1
0.5
0
-0.5
-1
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
Force (F)

(b)


Response (x)
1
0.5
0
-0.5
-1
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
Force (F)

(c)

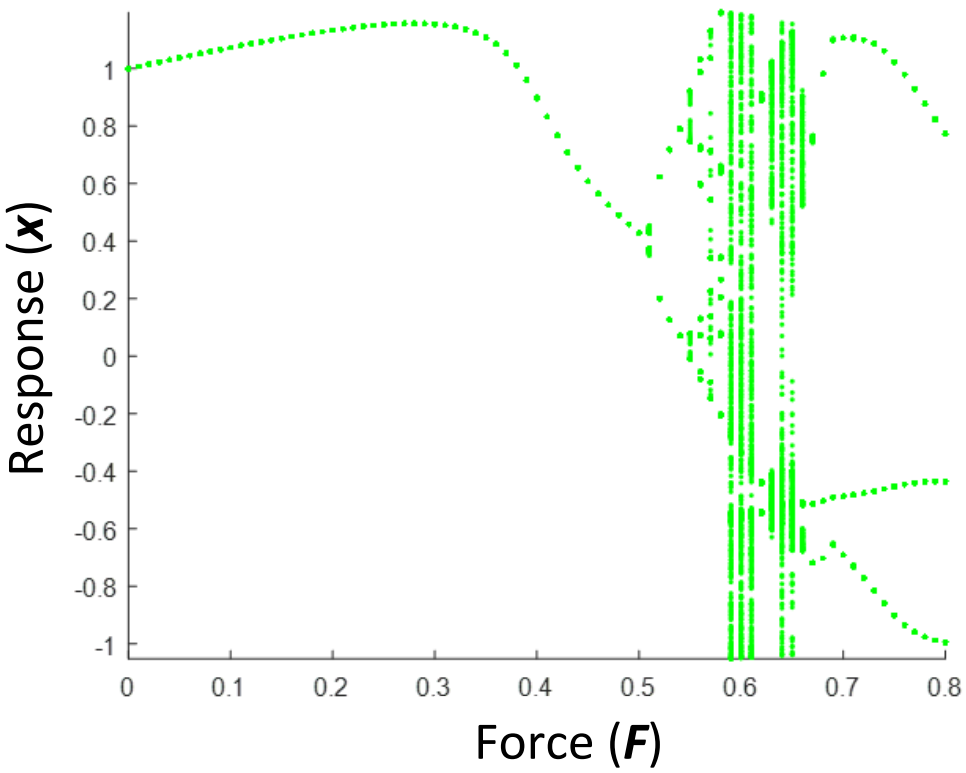

Response (x)
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
Force (F)

Figure S2