Supporting information

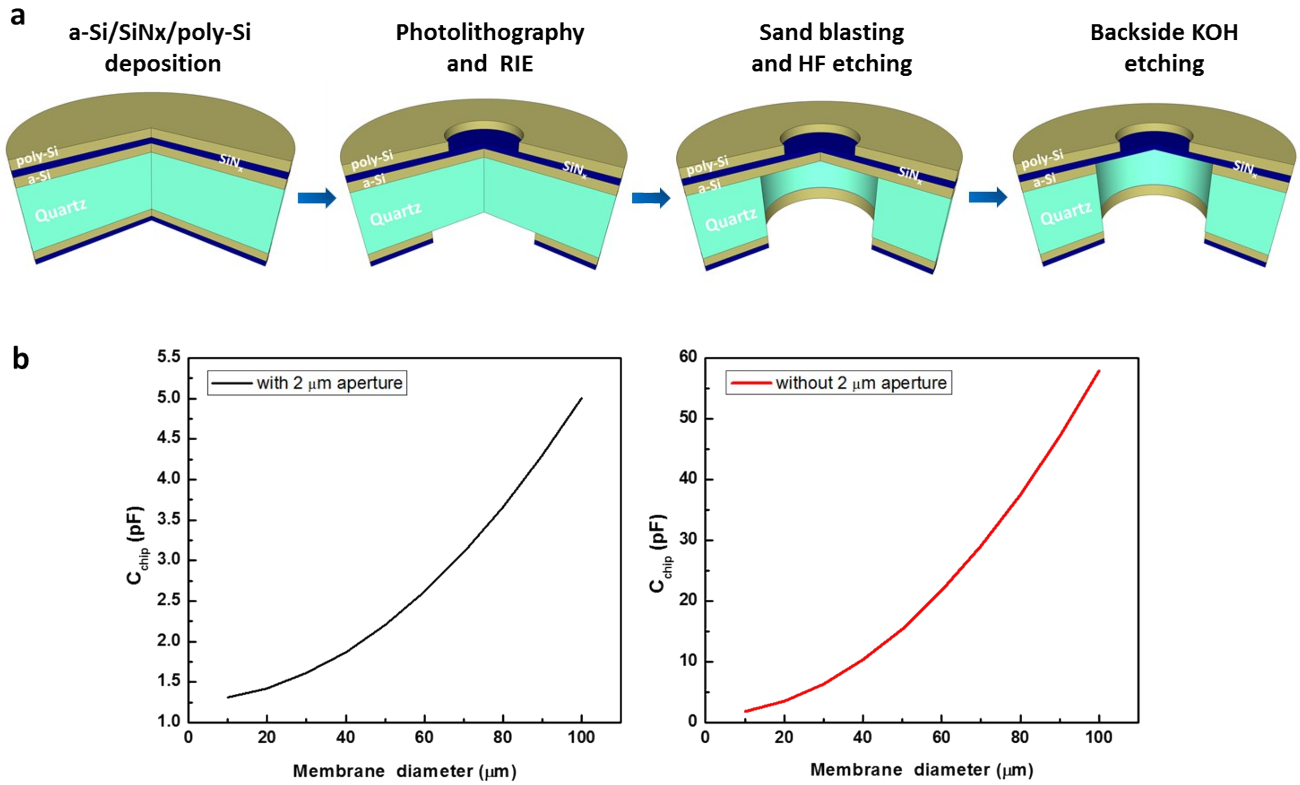
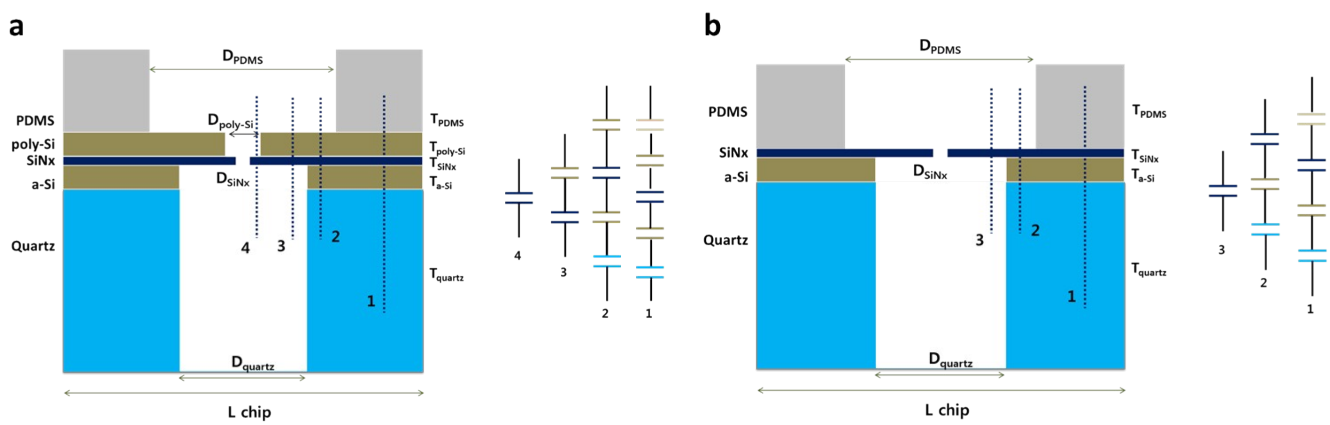


Figure S1. (a) Overall fabrication process of a transfer-free nanopore platform based on a quartz substrate. The specific geometry is described in Figure S2. A 100-nm-thick SiN_x layer is deposited by LPCVD and this layer is thinned down to sub-20 nm thickness by RIE etching and is later used as the active membrane. (b) The calculated chip capacitance as a function of the opening diameter of the active membrane with (left) and without (right) a 2 μm confinement on the active membrane



c

	Dielectric constant		Chip size		Diameter		Thickness
PDMS	2.55	Chip	5 mm x 5 mm	Quartz	10 ~ 100 μm	Quartz	300 μm
LP SIN	8.15			a-Si	100 μm	a-Si	200 nm
Si	11.5			pore size	5 nm	SiN	10 nm
Quartz	4.35			PDMS	3 mm	PDMS	1 mm
				poly-Si	2 μm	poly-Si	200 nm

Figure S2. (a) Schematic of a quartz-based chip with a poly-Si supporting layer. To calculate the chip capacitance, the chip structure was simplified into a capacitor circuit model. The labeled vertical region is the series connection of the capacitance and the total capacitance is calculated by parallel connection of the capacitance of each region. (b) Schematic of a quartz-based chip without a poly-Si supporting layer. The capacitance calculation procedure is similar to that in panel a. (c) The specific chip parameters including the dielectric constant of each material and the geometry of each layer.

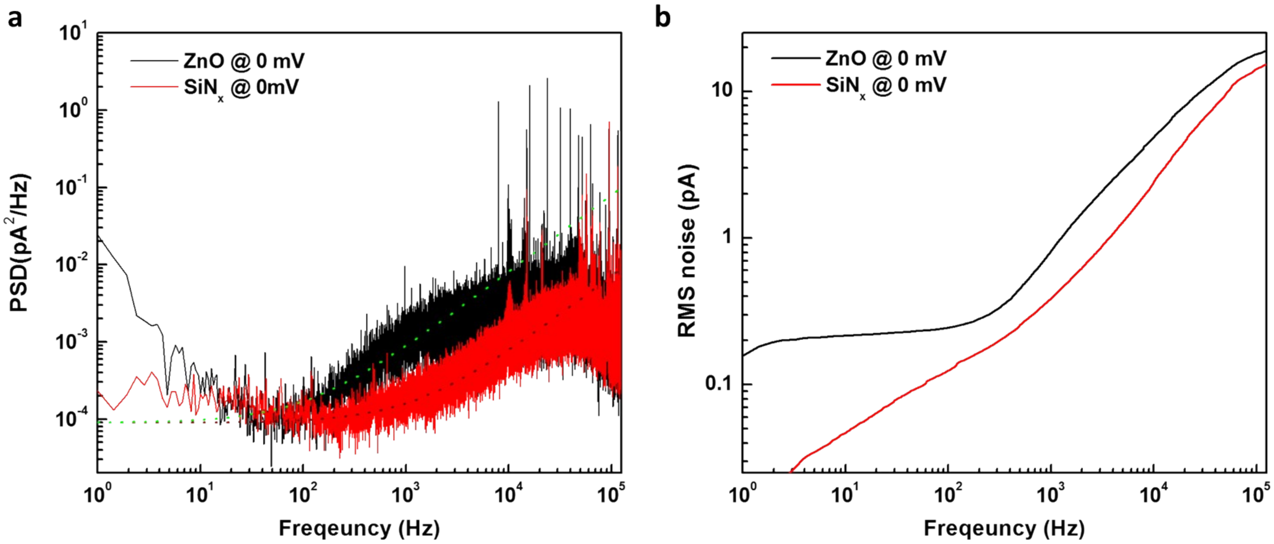


Figure S3. (a) Power spectral densities of ZnO and SiN_x nanopore devices with similar conductance (G ~ 7 nS) at 0 mV. The dotted lines are the fitting lines of thermal noise and dielectric noise. (b) RMS noise vs. frequency plots corresponding to panel a. RMS noise is calculated by the integration of PSD (S_I) over frequency according to the following relation, $I_{RMS} = \sqrt{\int S_I df}$.

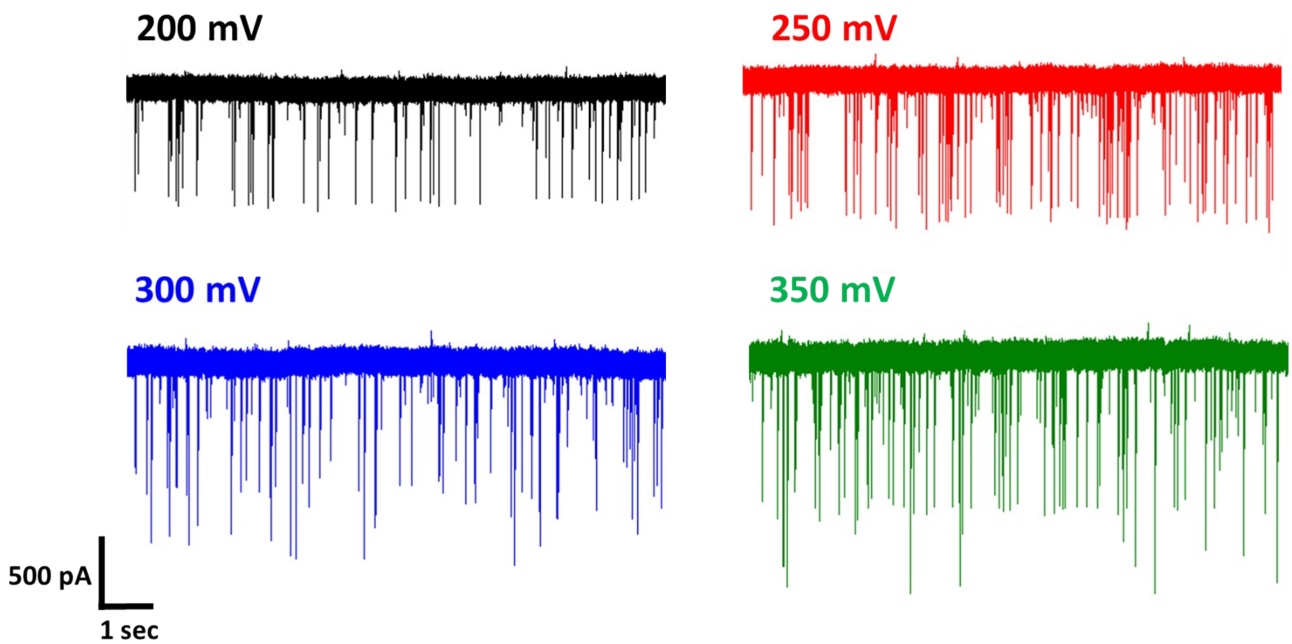


Figure S4. Continuous 10-s ionic current traces for 1 kbp dsDNA translocation through 4-nm-diameter ZnO nanopores in a 1 M KCl electrolyte solution with a TE buffer (pH 8.0) and a low pass bias filter at 100 kHz in the voltage range of 200–350 mV.

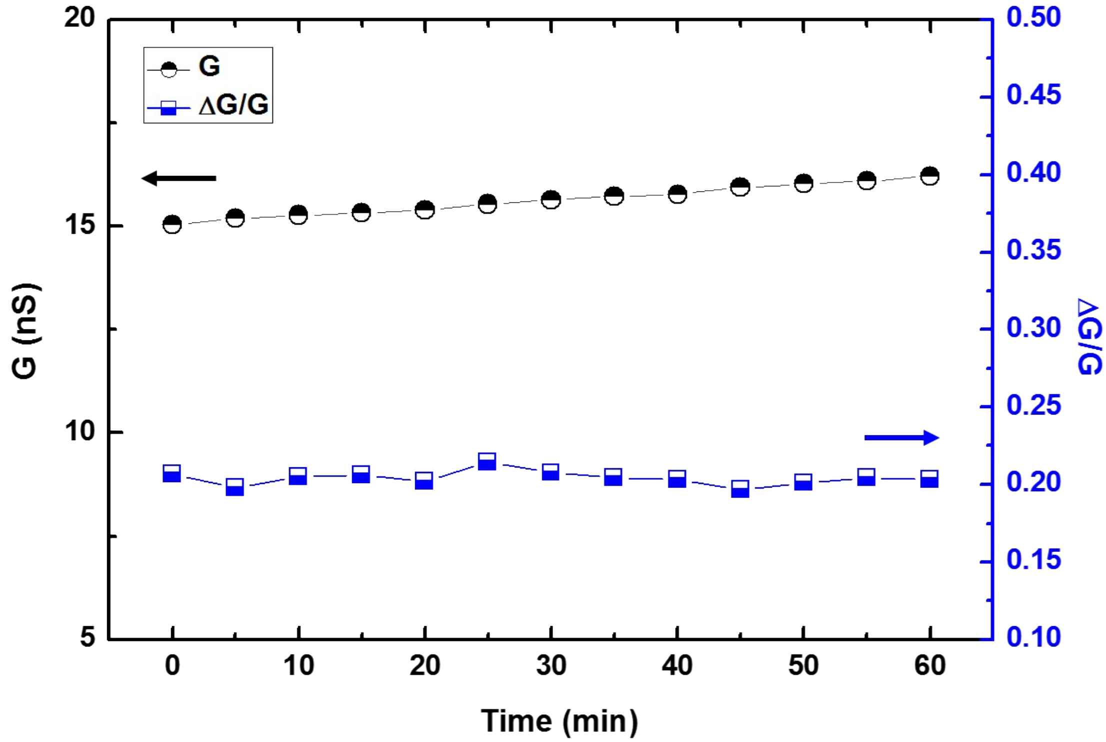


Figure S5. Pore conductance G (black, left axis) and ΔG/G ratio (blue, right axis) data with respect to the measurement time during 60 min for 4 nm ZnO nanopore in 1M KCl + TE buffer (pH 8.0) condition.

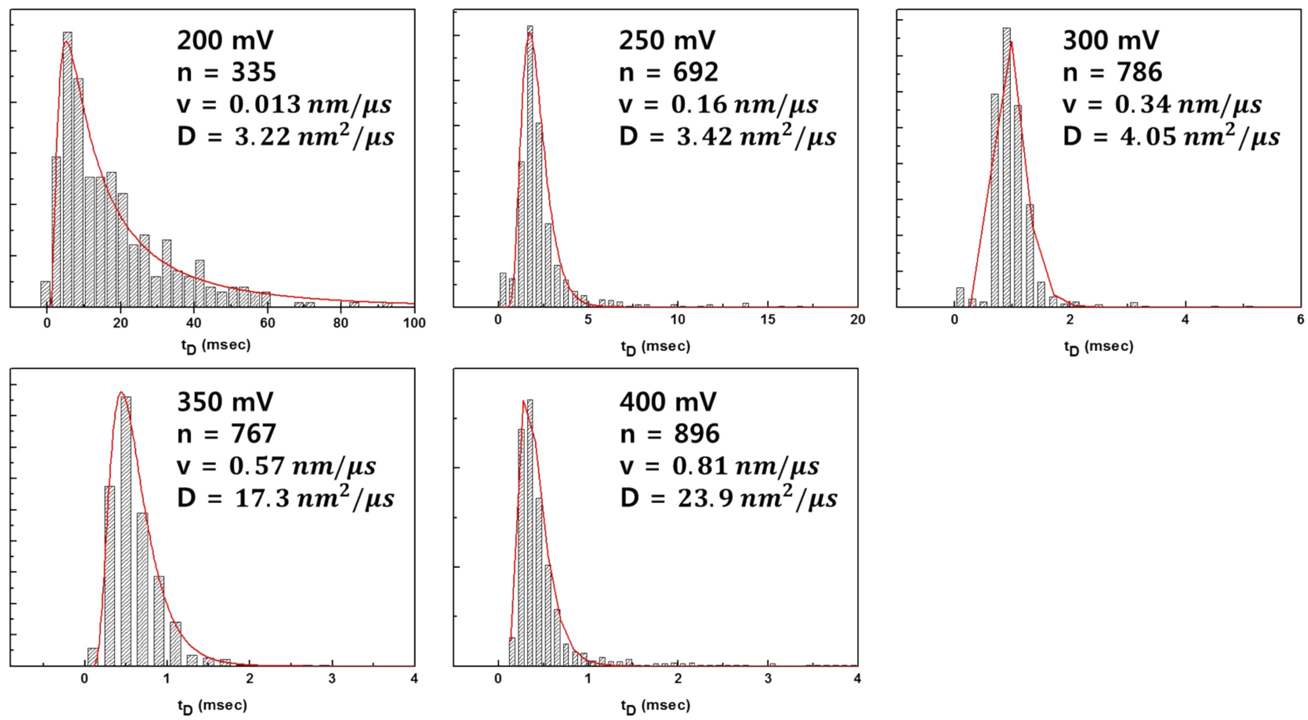


Figure S6. Histograms of dwell time for 1kbp dsDNA translocation through a 4-nm-diameter ZnO nanopore in the 200–400 mV applied voltage range. The solid lines are the fitting lines for the 1D Fokker-Planck model used to calculate the drift velocity and the diffusion coefficient.

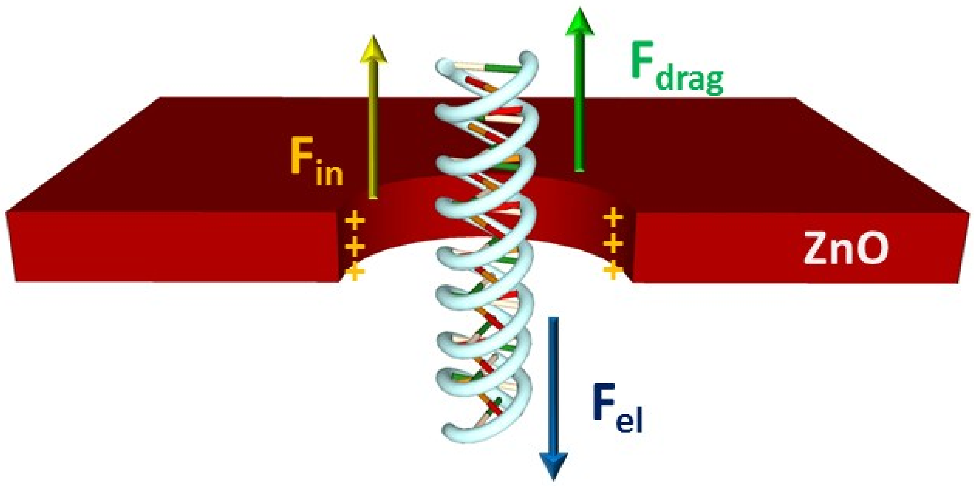


Figure S7. Scheme of a typical dsDNA translocation event through a positively charged ZnO nanopore along with the electrophoretic driving force (F_{el}), hydrodynamic drag force (F_{drag}), and surface frictional force (F_{in}) due to DNA-pore wall electrostatic interaction.

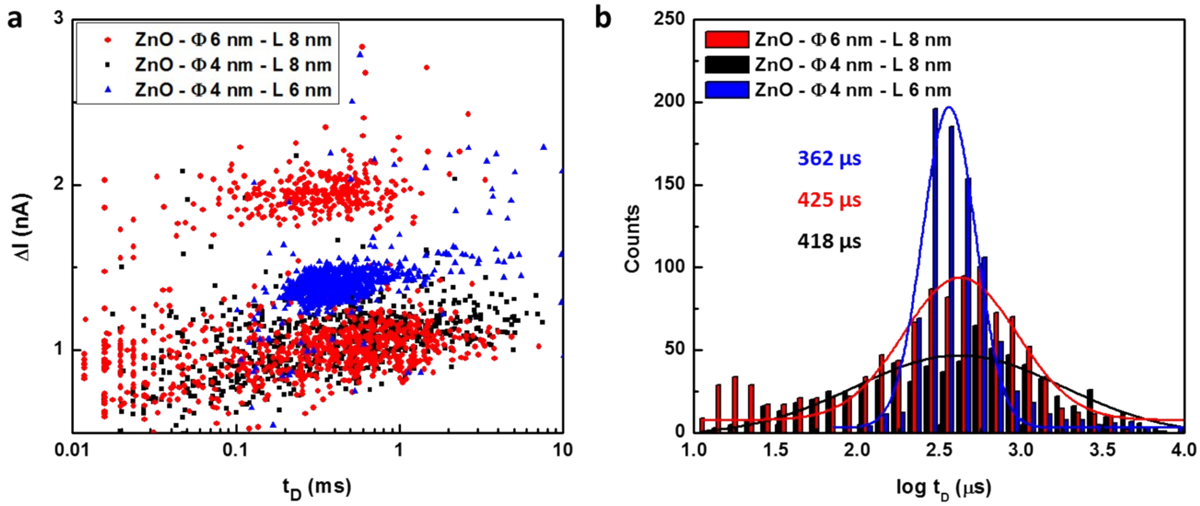


Figure S8. (a) Scatter plots of ΔI and t_D through ZnO nanopores of different diameters at 400 mV and (b) the corresponding histograms of log t_D.