Supplementary Materials

Effective electro-optic modulation in low-loss graphene-plasmonic slot waveguides

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S1. Theory and calculation of propagation loss

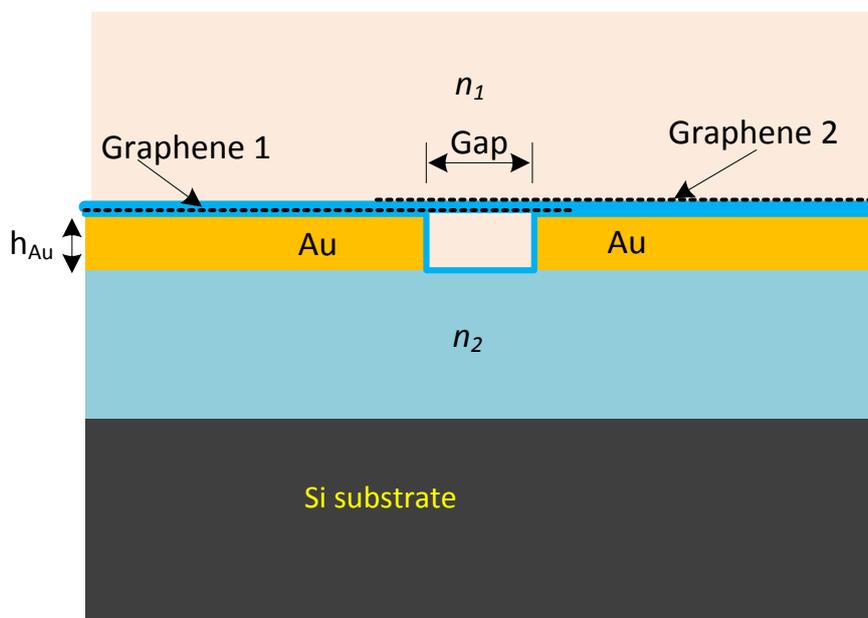The schematic of the designed graphene-plasmonic slot waveguide is shown in Fig. S1.

Fig. S1. Cross section of the designed graphene-plasmonic slot waveguide.

In order to accurately calculate the mode (including the leaky mode) of a plasmonic slot waveguide, the thickness of buried oxide layer (BOX) of the silicon-on-insulator (SOI) wafer and silicon substrate has to be considered. The thickness of BOX layer is 3 µm. The thickness of the Au sheet h_{Au} that forms the plasmonic slot waveguide is varied. The Al_2O_3 between the graphene layer 1 and Au plasmonic slot waveguide is designed to be 5 nm thick, and the Al_2O_3 between the two layers of graphene sheet is designed to be 10 nm. The thickness of the graphene sheet is considered to be 0.5 nm, and the Fermi level E_f dependent complex dielectric constant ($\varepsilon_G = \varepsilon'_G + j\varepsilon''_G$) of graphene can be described under the random phase approximation and the Kramers-Kronig relations

$$
\begin{aligned}
\varepsilon'_G\left(E_p\right) &= 1 + \frac{e^2}{8\pi E_p \varepsilon_0 d} \ln \frac{\left(E_p + 2\left|E_f\right|\right)^2 + \Gamma^2}{\left(E_p - 2\left|E_f\right|\right)^2 + \Gamma^2} - \frac{e^2}{\pi \varepsilon_0 d} \frac{\left|E_f\right|}{E_p^2 + \left(1/\tau\right)^2} \\
\varepsilon''_G\left(E_p\right) &= \frac{e^2}{4 E_p \varepsilon_0 d}\left[1 + \frac{1}{\pi}\left(\tan^{-1} \frac{E_p - 2\left|E_f\right|}{\Gamma} - \tan^{-1} \frac{E_p + 2\left|E_f\right|}{\Gamma}\right)\right] + \frac{e^2}{\pi\tau E_p \varepsilon_0 d} \frac{\left|E_f\right|}{E_p^2 + \left(1/\tau\right)^2}
\end{aligned}
\tag{Eq.S1}
$$

where E_p is the photon energy, d is the thickness of the two graphene layers, Γ is the inter-band broadening, and $1/\tau$ is the free carrier scattering rate. The refractive indices of Si, Al_2O_3, Au are considered to be 3.45, and 1.746 and $-131.94 + j12.65$, and the refractive indices of the upper cladding the substrate are denoted by n_1 and n_2 respectively. With the complex dielectric constant of graphene and Au, the complex effective refractive index ($n_{eff} = n_{eff,real} + jn_{eff,imag}$), the corresponding propagation is then obtained

$$
\alpha\left(dB/\mu m\right) = 2k_0 n_{eff,imag} \times 4.343 \times 10^{-6}
\tag{Eq.S2}
$$

where 4.343×10^{-6} is the constant for converting from m^{-1} to dB/µm.

S2. Study of coupling between silicon waveguide and plasmonic waveguide

The plasmonic slot waveguide can be effectively coupled with silicon waveguides by introducing inverse taper in the silicon waveguide tip, as shown in Fig. S2.
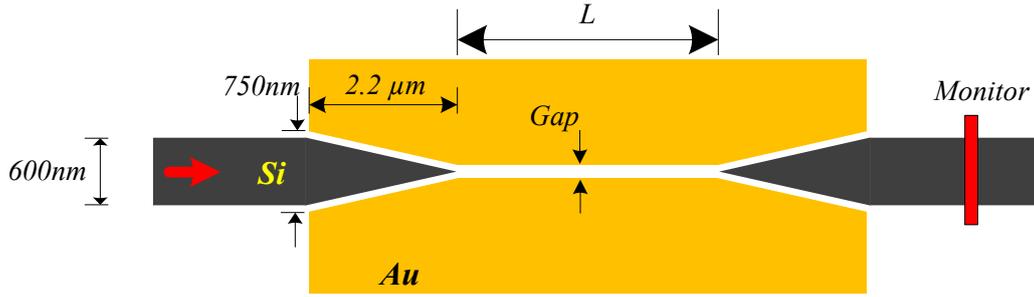
Fig. S2. Top view of the plasmonic slot waveguide coupled with silicon waveguides with inverse tip.

The transmission *T* is investigated by monitoring the output monitor calculated by three-dimensional Finite-difference time-domain method (3D-FDTD) simulation, and the coupling efficiency *a* between the silicon waveguide mode and the plasmonic leaky mode, can be express as

$$a = 10 \log \sqrt{T}$$

(Eq.S3)

where *L* = 0 μm is considered. Fig. S3(a) shows the calculated coupling efficiency (CE) as a function of coupling gap for different Au thicknesses. The coupling efficiency decreases as plasmonic gap increases. Increasing the Au thickness slightly increases the coupling efficiency. A highest CE of ~-0.86 dB can be achieved for small plasmonic gap of 80 nm, which may be challenge to fabricate. A CE of -1.06 dB and -1.32 dB is expected for plasmonic gap of 120 nm and 150 nm with Au thickness of 90 nm, respectively. This coupling configuration is also quite fabrication tolerant. Fig. S3(b) presents the CE as a function of misalignment between the silicon waveguide and plasmonic slot waveguide, showing that a misalignment of 45 nm and 60 nm misalignment tolerance is expected for plasmonic gap of 120 nm and 150 nm, respectively.
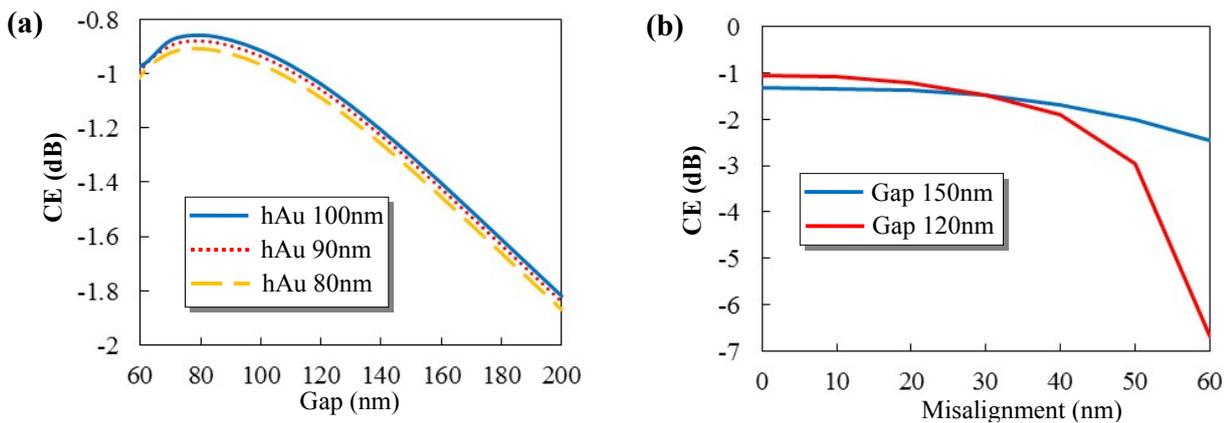

Fig. S3. (a) 3D FDTD calculated CE between a silicon waveguide and plasmonic slot waveguide as a function of plasmonic gap for different Au thickness. (b) 3D FDTD calculated CE as a function of alignment error for different plasmonic gap size.

S3. Fabrication process

The details of the fabrication process are shown in Fig. S4. The top silicon of a commercial SOI wafer was first thinned down to 90 nm in order to obtain a comparable thickness of the Au plasmonic slot waveguide (Fig. S4(i)~S4(ii)) by inductively coupled plasma (ICP) etching (STS Advanced Silicon Etcher). After that, standard SOI processing, including e-beam lithography (EBL, JEOL JBX-9300FS, e-beam resist: ZEP520A) and ICP etching, was first used to fabricate the etched silicon waveguides (Fig. S4(iii)~S4(iv)). Then the plasmonic slot waveguide was fabricated by a second EBL followed by Au metal deposition and liftoff process (Fig. S4(v)~S4(vii)). After that, the whole chip was coated with 5 nm Al_2O_3 deposited by Atomic Layer Deposition (ALD) (Fig. S4(viii)) in order to isolate the contact between the Au plasmonic slot waveguide and graphene layer 1 that will be transferred later. At the same time, AZ5214E photoresist was spin-coated onto the graphene covered copper foil and baked at 90 °C for 1 min (Fig. S4(ix)~Fig. S4(x)). Following that, AZ5214E/graphene membrane was obtained by wet-etching away the copper foil in a $Fe(NO_3)_3/H_2O$ solution, and transferred onto the silicon chip (Fig. S4(xi)~S4(xii)). Finally, the AZ5214E was dissolved in acetone and wet transfer of the graphene layer 1 was finished (Fig. S4(xiii)~S4(xiv)). The graphene coverage area was then defined by standard UV lithography and followed by oxygen plasma etching and resist removing (Fig. S4(xv)~S4(xvii)). The contact for graphene was then fabricated by standard UV lithography followed by Au/Ti deposition and liftoff process (Fig. S4(xviii)~S4(xx)). After that, 1 nm Al was deposited on the chip, and oxidized to Al_2O_3 in air. This native Al_2O_3 layer will be seed layer for the further Al_2O_3 deposition in ALD machine. Eventually, 10 nm Al_2O_3 was obtained (Fig. S4(xxi)). The graphene layer 2 was wet-transferred with the same transferring process (Fig. S4(xxii)~S4(xxvii)). The coverage area of graphene layer 2 was then defined by UV lithography followed by oxygen plasma etching and resist removing (Fig. S4(xxviii)~S4(xxx)). Finally, the contact for graphene layer 2 was fabricated by UV lithography followed by Au/Ti deposition and liftoff process (Fig. S4(xxxi)~S4(xxxiii)).
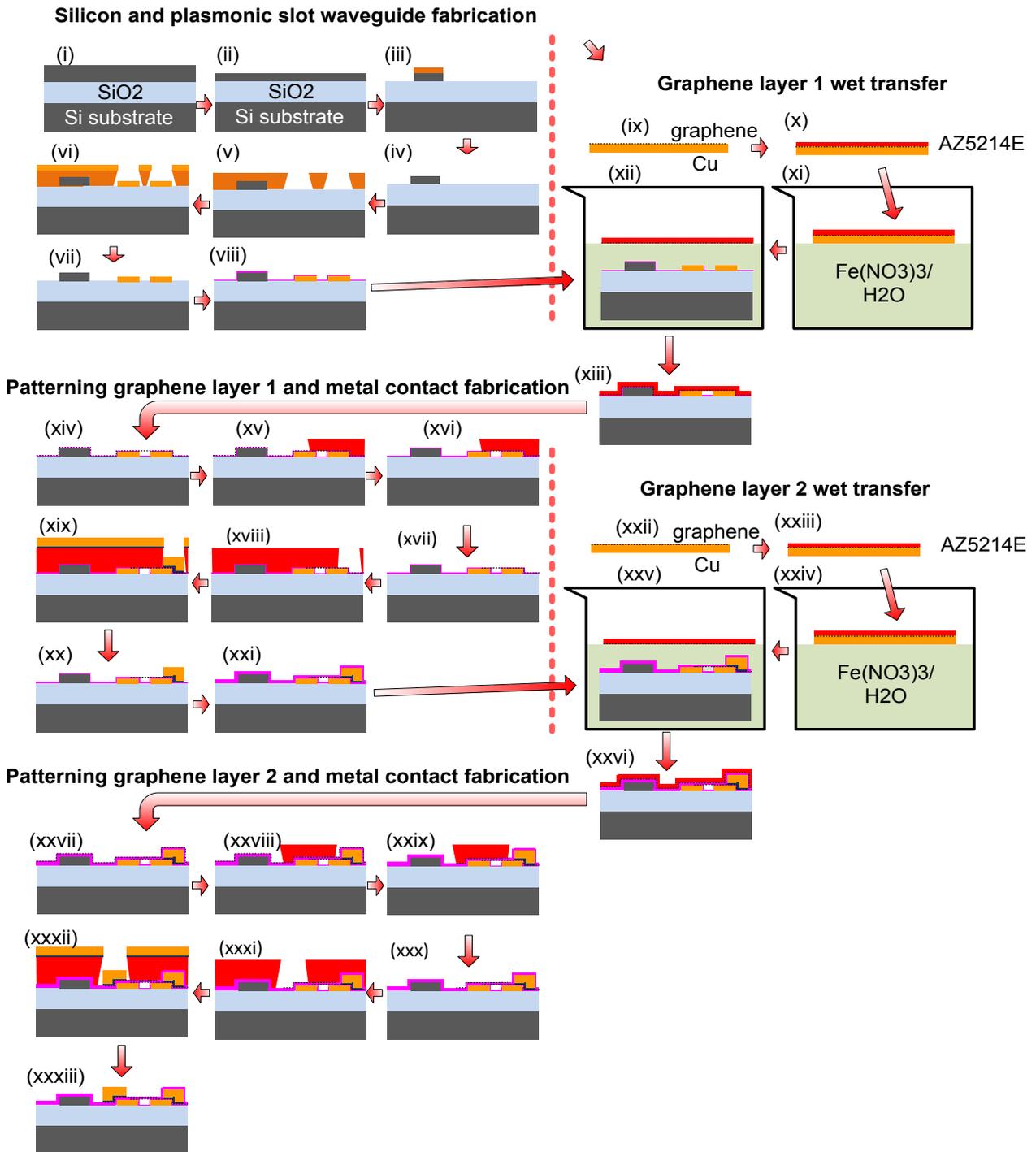
Silicon and plasmonic slot waveguide fabrication

(i) SiO2 / Si substrate

(ii) SiO2 / Si substrate

(iii)

(iv)

(v)

(vi)

(vii)

(viii)

Graphene layer 1 wet transfer

(ix) graphene / Cu

(x) AZ5214E

(xi) Fe(NO3)3/ H2O

(xii)

(xiii)

Patterning graphene layer 1 and metal contact fabrication

(xiv)

(xv)

(xvi)

(xvii)

(xviii)

(xix)

(xx)

(xxi)

Graphene layer 2 wet transfer

(xxii) graphene / Cu

(xxiii) AZ5214E

(xxiv) Fe(NO3)3/ H2O

(xxv)

(xxvi)

Patterning graphene layer 2 and metal contact fabrication

(xxvii)

(xxviii)

(xxix)

(xxx)

(xxxi)

(xxxii)

(xxxiii)

Fig.S4. Detailed fabrication process flow of the graphene-plasmonic slot waveguide based E/O modulator.

S4. Characterization setup

The experimental setup for measuring the graphene-plasmonic slot waveguide based E/O modulator is exhibited in Fig. S5. Light from a tunable laser source (TLS, ANDO AQ4321A) was polarization-tuned by a polarization controller (PC), and injected into the grating coupler which was designed on the TE mode. The

light output from the chip was coupled to the output fiber by a grating coupler, and detected by the optical spectral analyzer (OSA, AQ6317B). The electrical contacts for the two graphene layers were connected to a power supply (Keithley 238, High Current Source Measure Unit). In the E/O switching experiment, the square waveform is generated by a waveform generator (Stanford Researcher Systems Inc., Model DG 535, Four Channel Digital Delay/Pulse Generator).
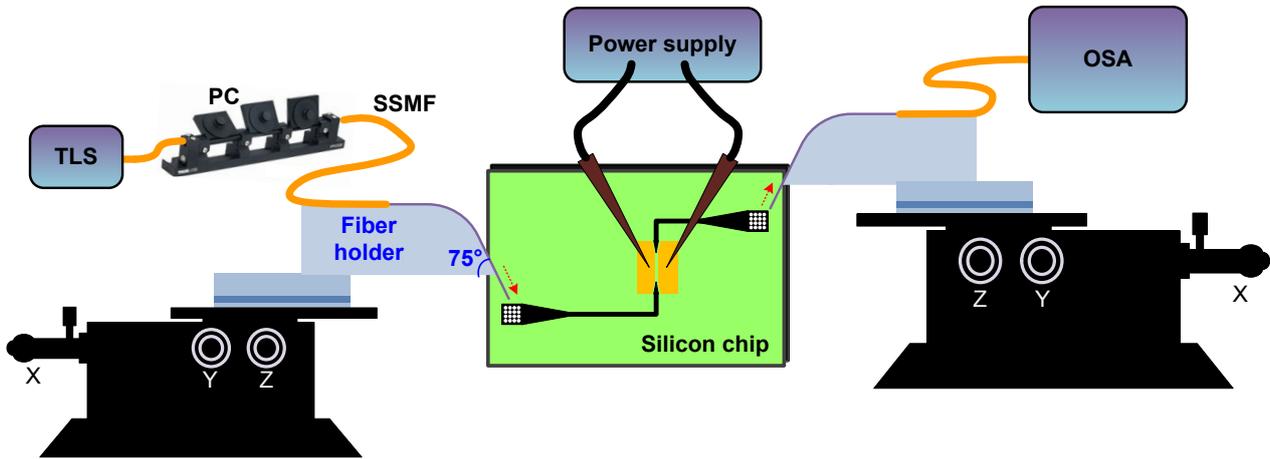

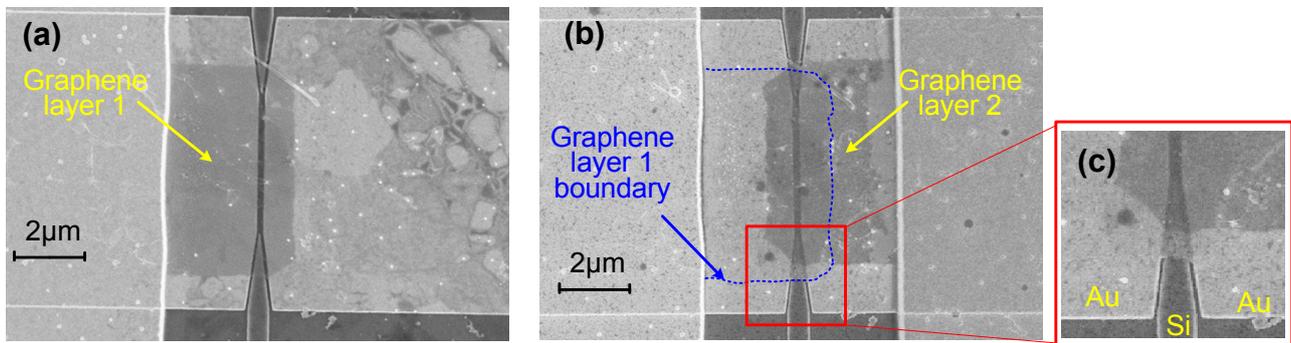**Fig. S5. Experimental setup for characterizing graphene-silicon devices.**

Fig. S6. Scanning electron microscope (SEM) images of fabricated graphene-plasmonic slot waveguide after (a) contact fabrication on the graphene layer 1, corresponding to step Fig. S5(xxi). and (b) contact fabrication on the graphene layer 2, corresponding to the final step Fig. S5(xxxiii). (c) SEM image of the zoom-in of the coupling area between silicon waveguide with inverse taper and plasmonic slot waveguide, clearly indicating good coverage by two graphene layers.