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Supporting Information for

Floating-Gate Controlled Programmable Non-volatile Black Phosphorus PNP Junction Memory

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METHODS

Fabrication of BP/h-BN/Graphene Heterostructure Devices. Few-layer BP, h-BN, graphene flakes were all prepared using a mechanical exfoliation method from bulk crystals. Highly-doped silicon wafer with a 300-nm thick thermal oxide film was the substrate. The assembly of the few-layer flakes was processed with a dry transfer procedure. A few-layer graphene flake was first exfoliated on the prepared SiO_2 substrate using 3M Scotch tape. A few-layer h-BN flake was transferred on a transparent PDMS film using a similar method. With the help of an optical microscope, the h-BN flake was aligned on the graphene. After a slight press, the h-BN was transferred to the desired position due to the affinity difference between the PDMS and SiO_2. A few-layer BP flake was aligned on the obtained h-BN/graphene heterostructure using a similar method. Thus, the BP/h-BN/graphene heterostructure was formed. Finally, e-beam lithography (EBL) was used to define Au/Cr (50 nm/5 nm) electrodes on the produced BP/h-BN/graphene heterostructure.

Characterizations. Keithley 4200-SCS semiconductor analyzer was used to characterize the electrical properties of the devices in a probe station with a high vacuum of 10^{-4} Pa. Atomic force microscope (AFM, DIMENSION edge) was used to determine the thickness of BP, graphene, and h-BN flakes under a tapping mode. Raman measurement was carried out with a Horiba Jobin Yvon LabRAM HR Raman system. The excitation is provided by a 514-nm laser with a power of 5 mW.

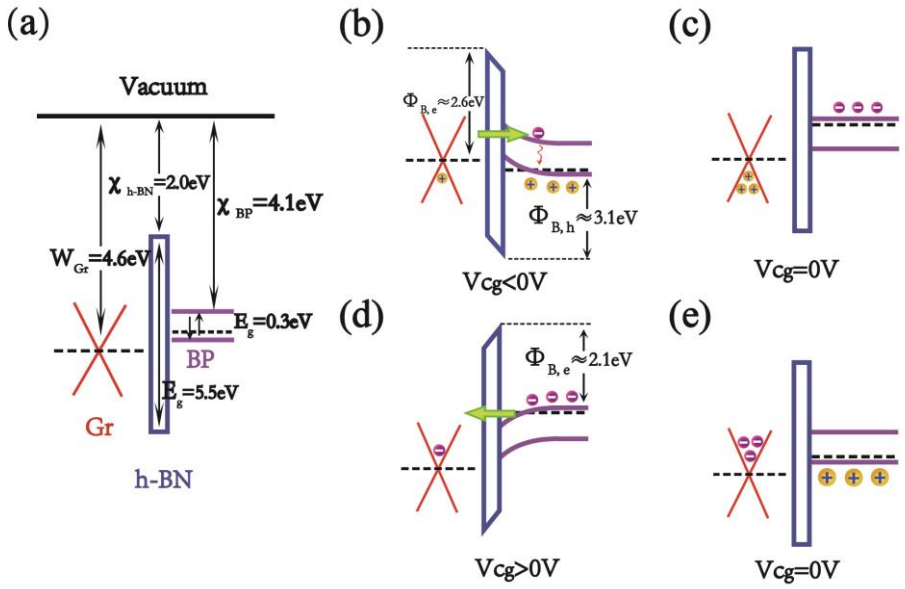

Fig. S1. Energy band diagram of the graphene/h-BN/BP heterostructure. (a) Flat energy band structure, where χ and Eg represent the electron affinity and bandgap of semiconductors, respectively, and W represents the work function of graphene. (b) Schematic energy band diagram of the heterostructure under a negative control gate voltage and (c) while the negative control gate voltage is removed. (d) Schematic energy band diagram of the heterostructure under a positive control gate voltage and (e) while the positive control gate voltage is removed.

Fig. S1 shows the detailed energy band diagram of the graphene/h-BN/BP heterostructure. Previous studies have demonstrated that few-layer graphene is a semi-metal with a work function of 4.6 eV.[1] For few-layer h-BN, the electron affinity and the band gap are 2.0 eV and 5.5 eV, respectively.[2] For few-layer BP, they are 4.1 eV and 0.3 eV, respectively.[3] By using the energy band diagram, we can explain how the device works at different states.

When a negative voltage (-30V) is applied on the control gate, holes are induced in the BP due to the fringing field effect.[4] At the same time, an electrical potential from the BP to the control gate is produced. As shown in Fig. S1b, the barrier height for holes to tunnel through the h-BN layer from the BP to graphene is 3.1 eV, but the barrier height for electrons to tunnel through the h-BN layer from the graphene to BP is 2.6 eV. So under such condition, it is reasonable to conclude that the tunneling of electrons from the graphene to BP dominates the tunneling process. Driven by the outer electric field from the control gate to the channel, the electrons will tunnel though the h-BN layer from the bottom graphene to the channel, leading to the fact that the floating gate becomes positively charged. While the control gate voltage is removed, inversion electrons will be attracted in the BP channel (Fig. S1c).

When a positive voltage (+30V) is applied on the control gate, electrons are induced in the BP. At the same time, an electrical potential from the control gate to BP is produced. As shown in Fig. S1d, the barrier height for electrons to tunnel through the h-BN layer from the BP to graphene is 2.1 eV. Driven by the outer electric field from the control gate to the channel, the electrons will tunnel though the h-BN layer to the bottom graphene. The electrons trapped in the graphene will further attract inversion holes in the BP channel (Fig. S1e).

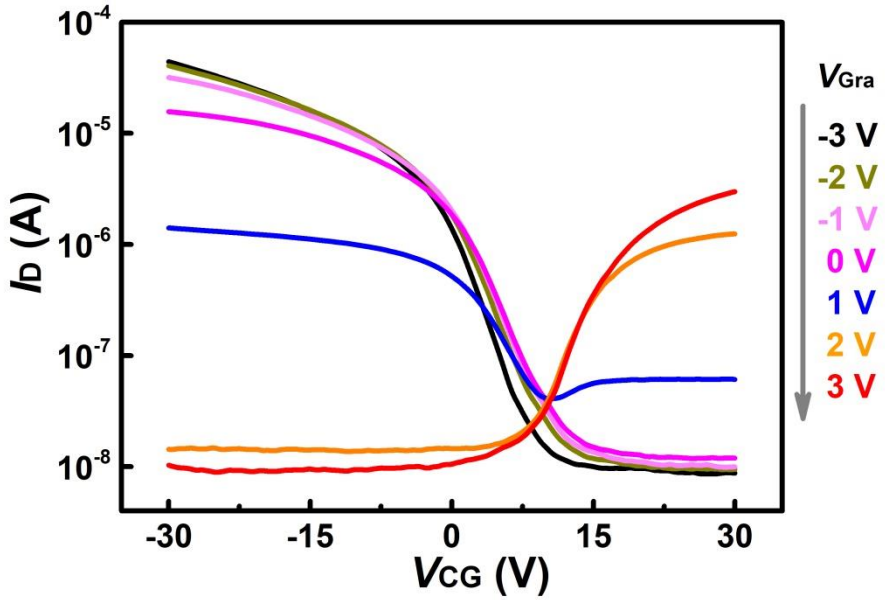

Fig. S2 Double-gate BP field-effect transistor. When both the floating gate (graphene) and the control gate (silicon) are applied with voltages, the device operates as a double-gate field-effect transistor. The graphene gate would induce charge carriers in M-BP and the silicon gate would induce charge carriers in E-BP. And if the charges induced by graphene gate and silicon gate are not equal, junction would form along the BP flake. Typically, when a negative voltage is applied on graphene, M-BP is highly p-doped and, under the control gate scanning voltage, the device will exhibit unipolar p-type FET behavior as the conduction in positive V_{CG} direction is suppressed by the $NP^{+}N$ junction formed in the BP flake. When a large positive voltage is applied on graphene, M-BP is n-doped and the device will exhibit unipolar n-type FET behavior as the conduction in negative V_{CG} direction is suppressed by the PNP junction formed in the BP flake.

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