Electronic Supplementary Material (ESI) for RSC Advances.

Supporting Information

Growth of Single Crystalline Cubic Structured Tin (II) Sulfide (SnS) Nanowires by Chemical Vapor Deposition

Devika Mudusu [1,2,#], Koteeswara Reddy Nandanapalli [1,3,#,*], Sreekantha Reddy Dugasani [3,#], Jang Won Kang[1,4], Sung Ha Park[3,*], and Charles W. Tu[1,5,*]

[1]Department of Nanobio Materials and Electronics, Gwangju Institute of Science and Technology, Gwangju-500712, Republic of Korea

[2]School of Advanced Materials Science & Engineering, Sungkyunkwan University, Suwon, Gyeonggi-do, 440746, South Korea

[3]Department of Physics, Sungkyunkwan University, Suwon 440746, South Korea

[4]Department of Emerging Materials Science, Daegu Gyeongbuk Institute of Science and Technology (DGIST), Daegu 42988, South Korea

[5]Department of Electrical and Computer Engineering, University of California, San Diego, La Jolla, CA 92093-0407, USA

SI1: Experimental setup of CVD system.

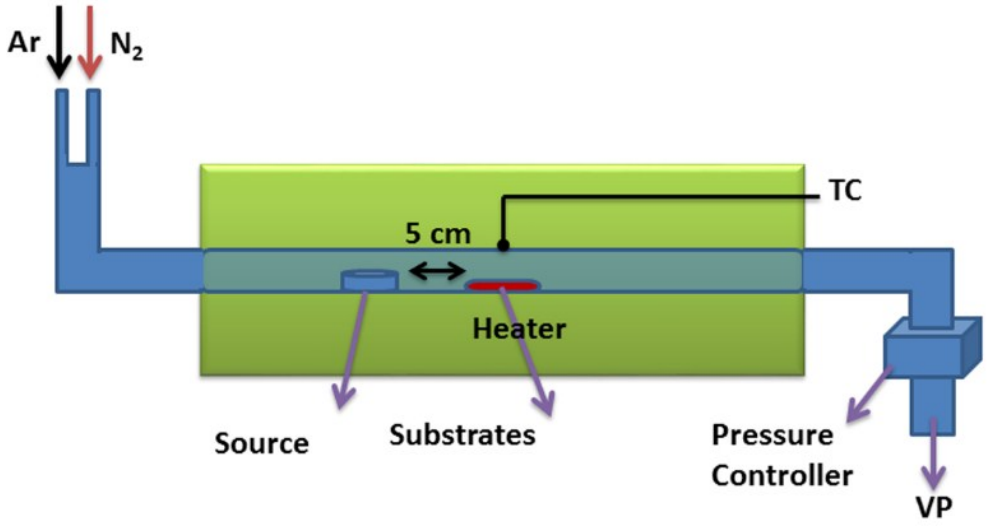

Fig. SI1: Schematic diagram of chemical vapor deposition system

SI2: Au catalysts coated on sapphire and Si substrates by e-beam evaporation.

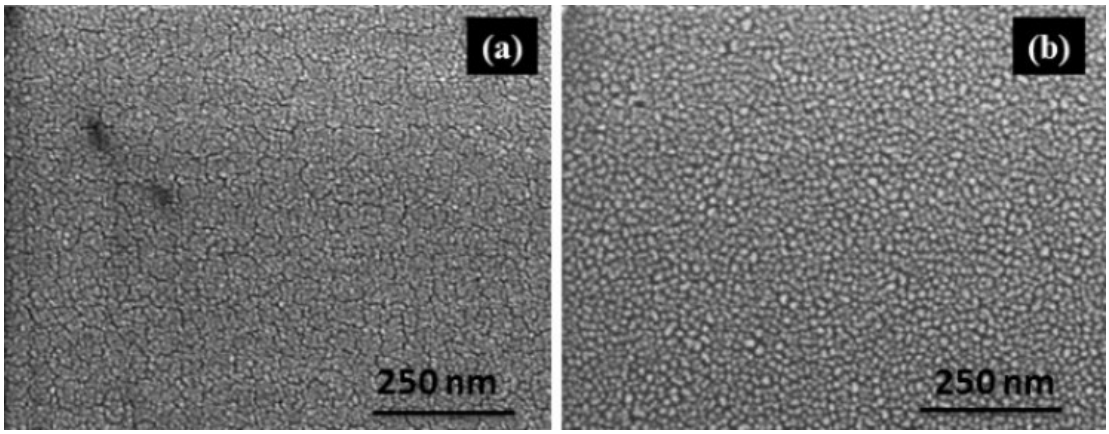

Fig. SI2: FESEM images of Au catalyst coated (a) sapphire and (b) Si substrates

SI3: SnS Nanostructures grown at different temperatures below 650 °C

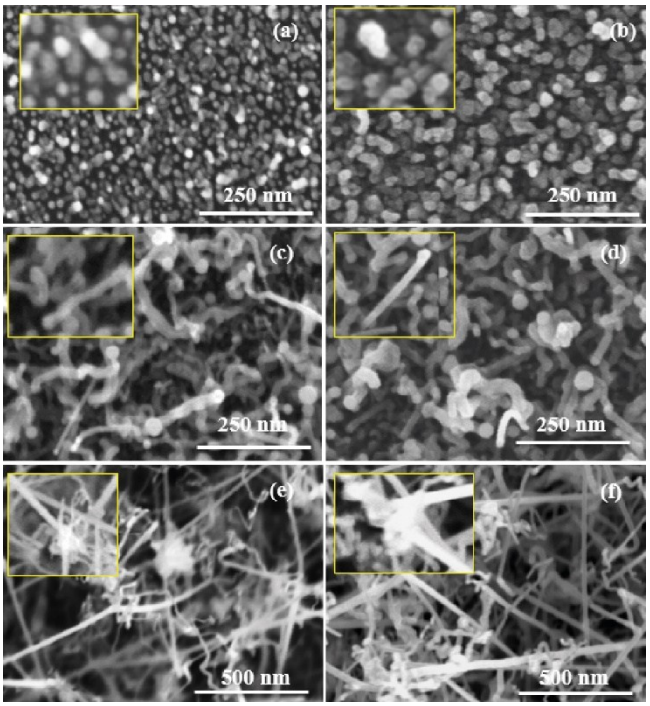

Fig. SI3: Figure 1: FESEM images of SnS nanostructures grown on sapphire (left column) and Si (right column) substrates at the growth temperature of (a, b) 500, (c, d) 550 and (e, f) 600 °C, respectively.

SI4: Surface morphology of SnS nanostructures grown on sapphire substrates at 600 °C.

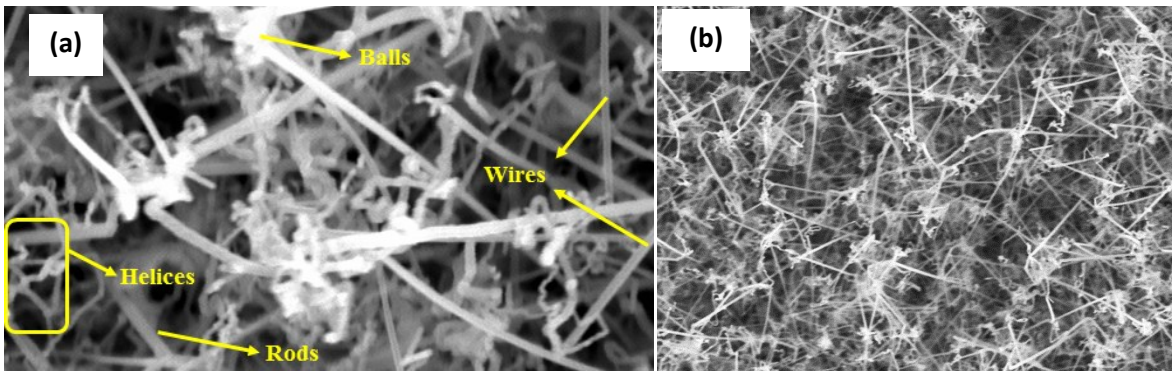

Fig. SI4: FESEM images of SnS nanostructures grown at 600 °C (a) high and (b) low magnification images (consists of different morphologies)

SI5: Surface morphology of SnS NWs grown on Si substrate at 650 ^{o}C

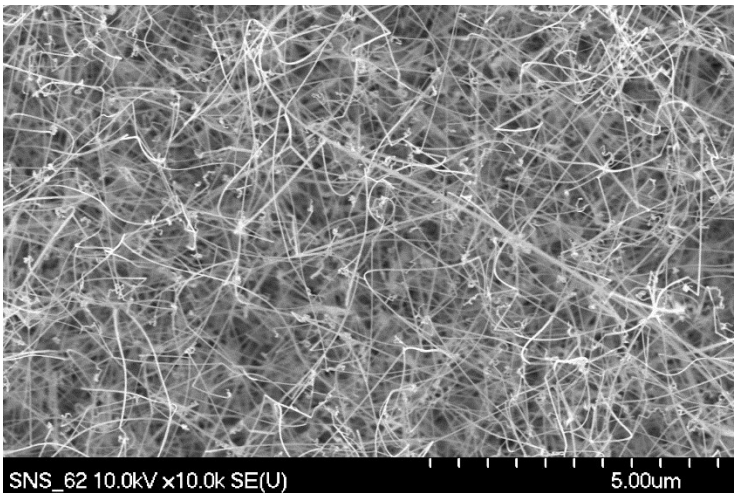

Fig. SI5: FESEM image of SnS NWs grown on Si substrate at 650 ^{o}C

SI6: SnS Nanostructures grown at different temperatures above 650 ^{o}C

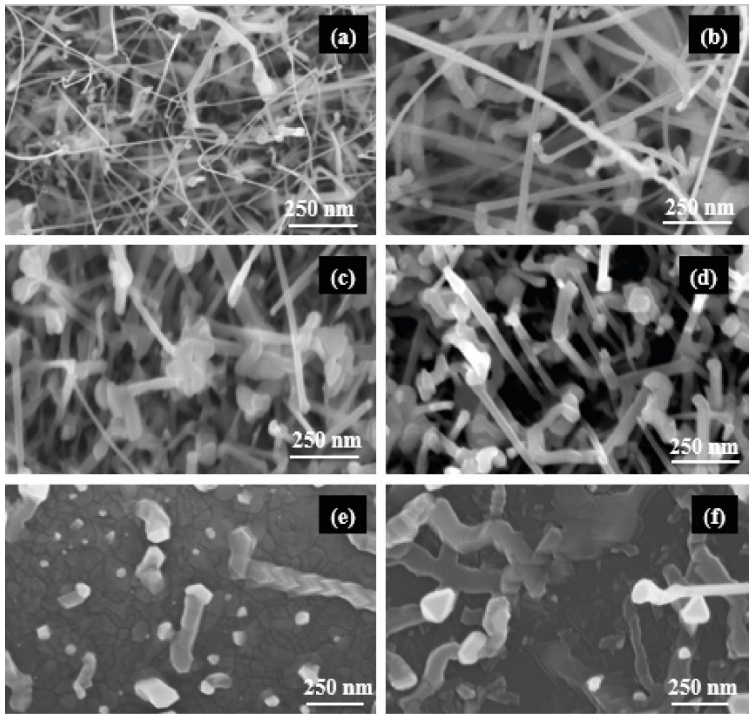

Fig. SI6: FESEM images of SnS nanostructures grown on sapphire (left column) and Si (right column) substrates at the growth temperature of (a, b) 700, (c, d) 800 and (e, f) 950 ^{o}C, respectively.

SI7: Diameters of SnS nanowires present on top surface of the structures, which were extracted by using ImageJ software for different samples grown at different temperatures.

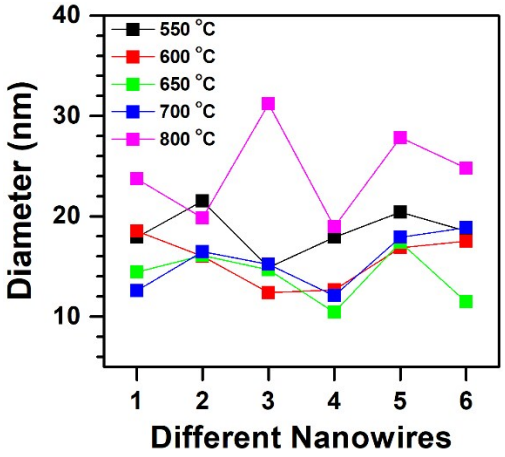

Fig. SI7: Variation of diameter of SnS nanowire as a function of different nanowires present on the top surface of the structures.

SI8: Chemical composition of SnS NWs grown at 650 °C.

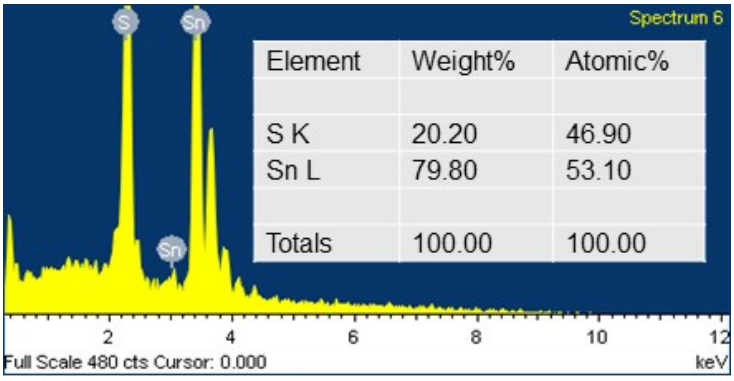

Fig. SI8: EDS spectrum of SnS NWs on Si substrates at the growth temperature of 650 °C

SI9: Calculation of lattice parameter(s) of SnS nanowires

From the standard geometric concepts, the following equation can be derived for a unit cell lattice consists of a, b, c as lattice constants, d as space between two consecutive atoms and h, k,

l are Miller indices.

$$\frac{1}{d^2}=\frac{h^2}{a^2}+\frac{k^2}{b^2}+\frac{l^2}{c^2}$$

For cubic structured lattice a=b=c, therefore, the above equation can be written as

$$\frac{1}{d^2}=\frac{1}{a^2}(h^2+k^2+l^2)$$

In the present study, the obtained d is 0.275 nm and thus, $a^2 = 4d^2$,

$\Longrightarrow$ a = 0.55 nm

= b=c.

SI10: Survey scan of the XPS spectrum of SnS nanowires

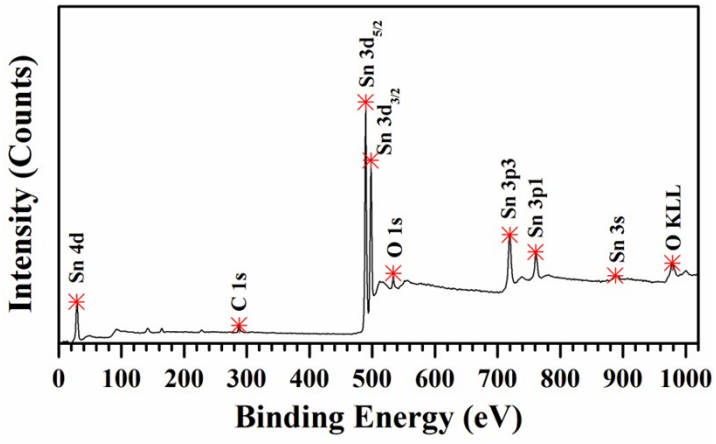

Fig. SI10: Survey scan of XPS spectrum of SnS nanowires grown on Si substrate at the growth temperature of 650 ^{o}C

SI11: SnS films on sapphire substrate at a growth temperature of 450 ^{o}C

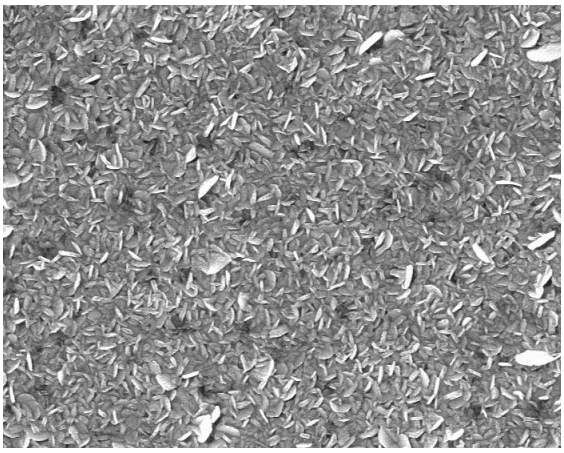

Fig. SI11: FESEM image of SnS films grown at the growth temperature of 450 ^{o}C