

ELECTRONIC SUPPLEMENTARY INFORMATION

Investigation of micro- and nanoscale barrier layer capacitance mechanisms of conductivity in $\text{CaCu}_3\text{Ti}_4\text{O}_{12}$ via Scanning Probe Microscopy technique

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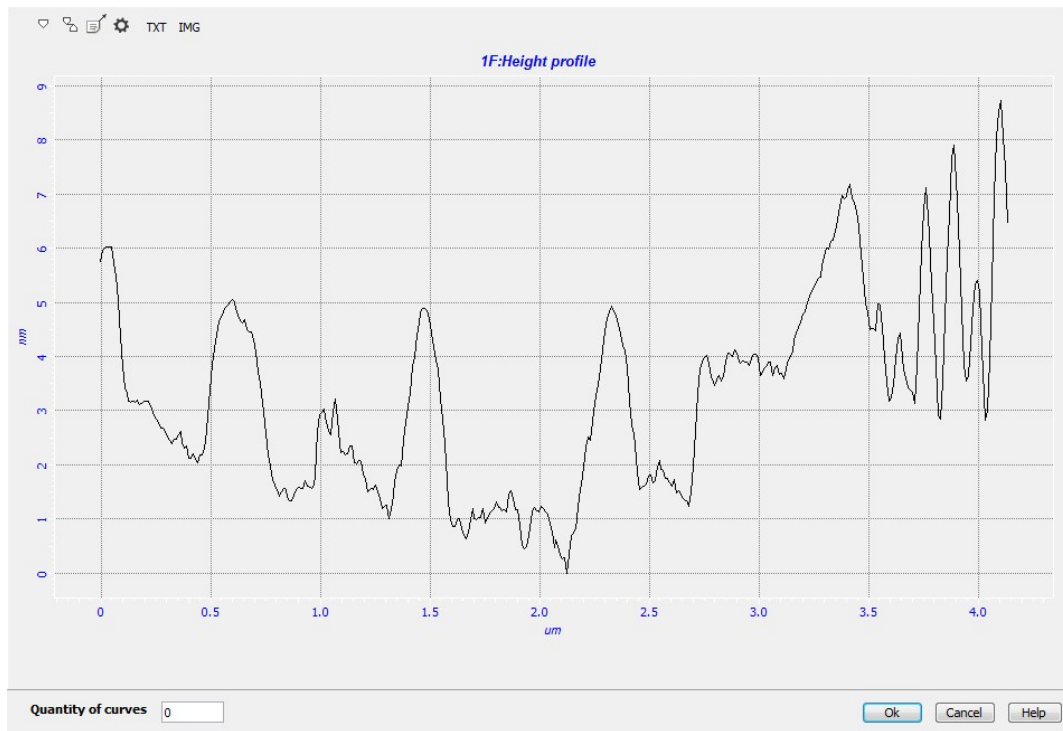
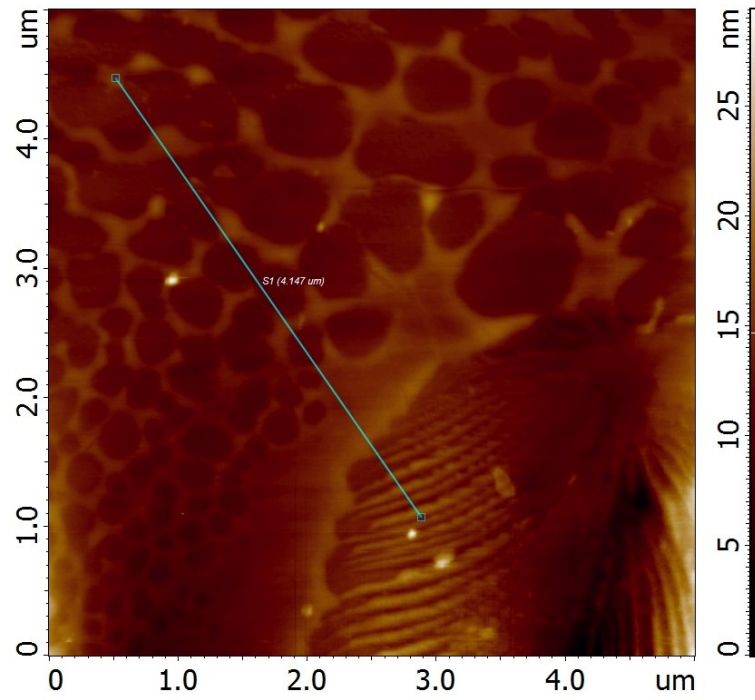


Figure 1. Surface topography of mechanically-polished CCTO sample and typical cross-section indicating the RMS roughness of around 5 nm.

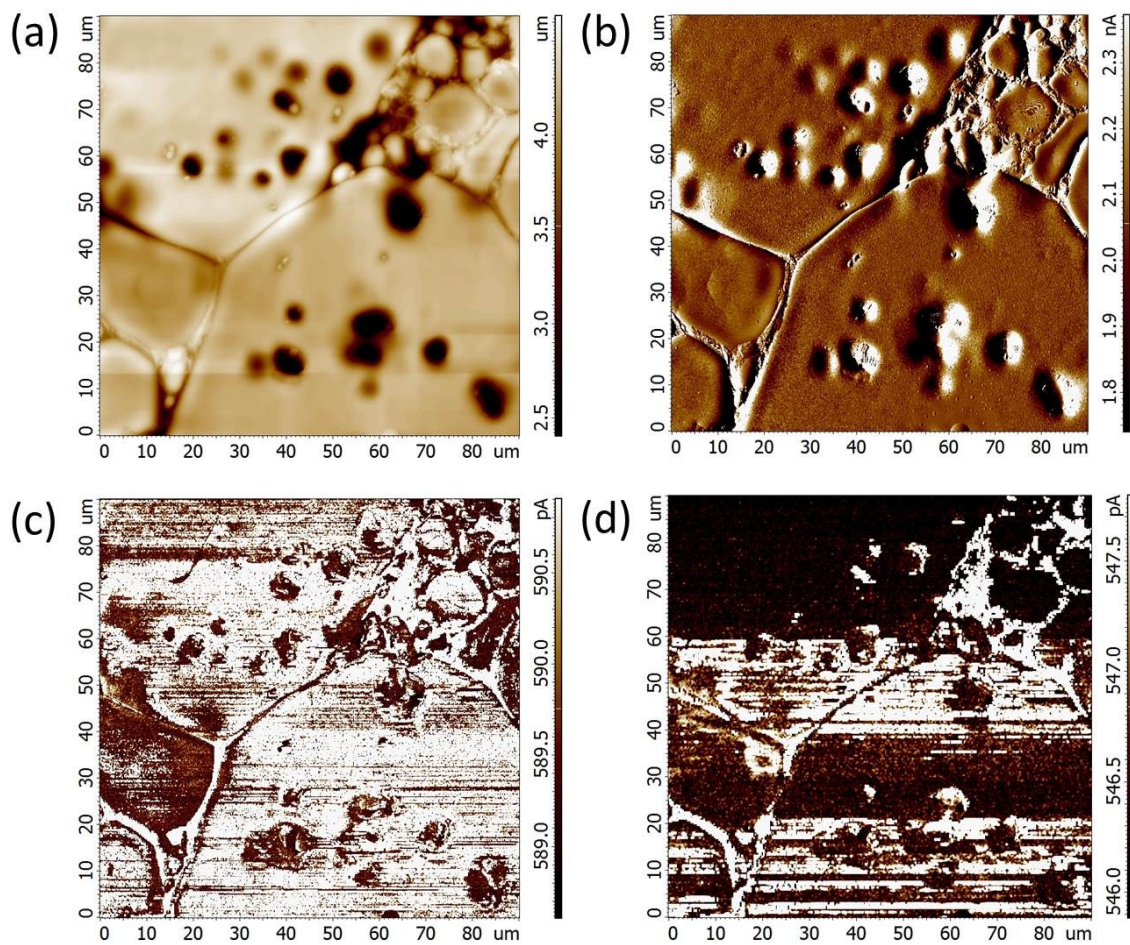


Figure 2. Topography (a), DFL response (b) and corresponding SR signal decay due to the degradation of the Pt/Ir coating: new tip (c), the same tip after 3 hours cycling at 0.1 Hz (512 x 512 pixels) (d).

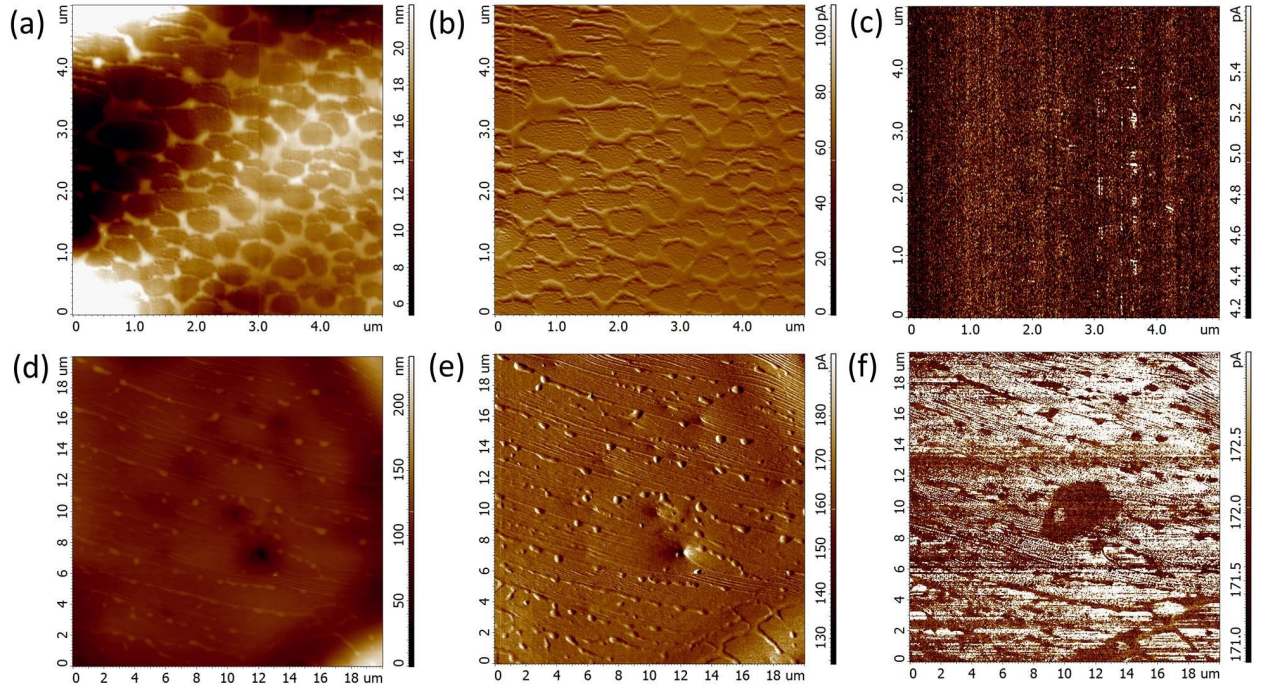


Figure 3. A comparison of the topographies (a, d), DFL responses (b, e) and corresponding current distributions (c, f) characteristic of the bump (upper part) and terrace-ledge (bottom part) domain structures (the notation is taken from Ref. 1).

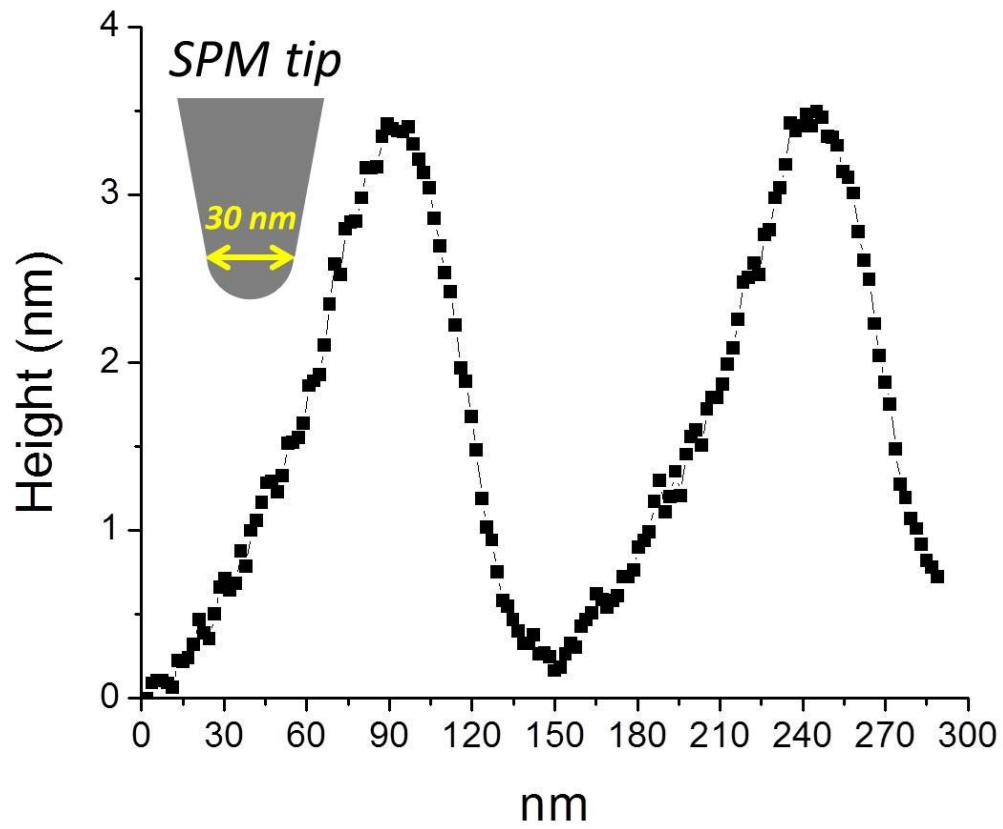


Figure 4. The size relation between the apex of the SPM probe and the typical roughness of the CCTO sample (the profile of terrace ledge 2 domain topography is presented).

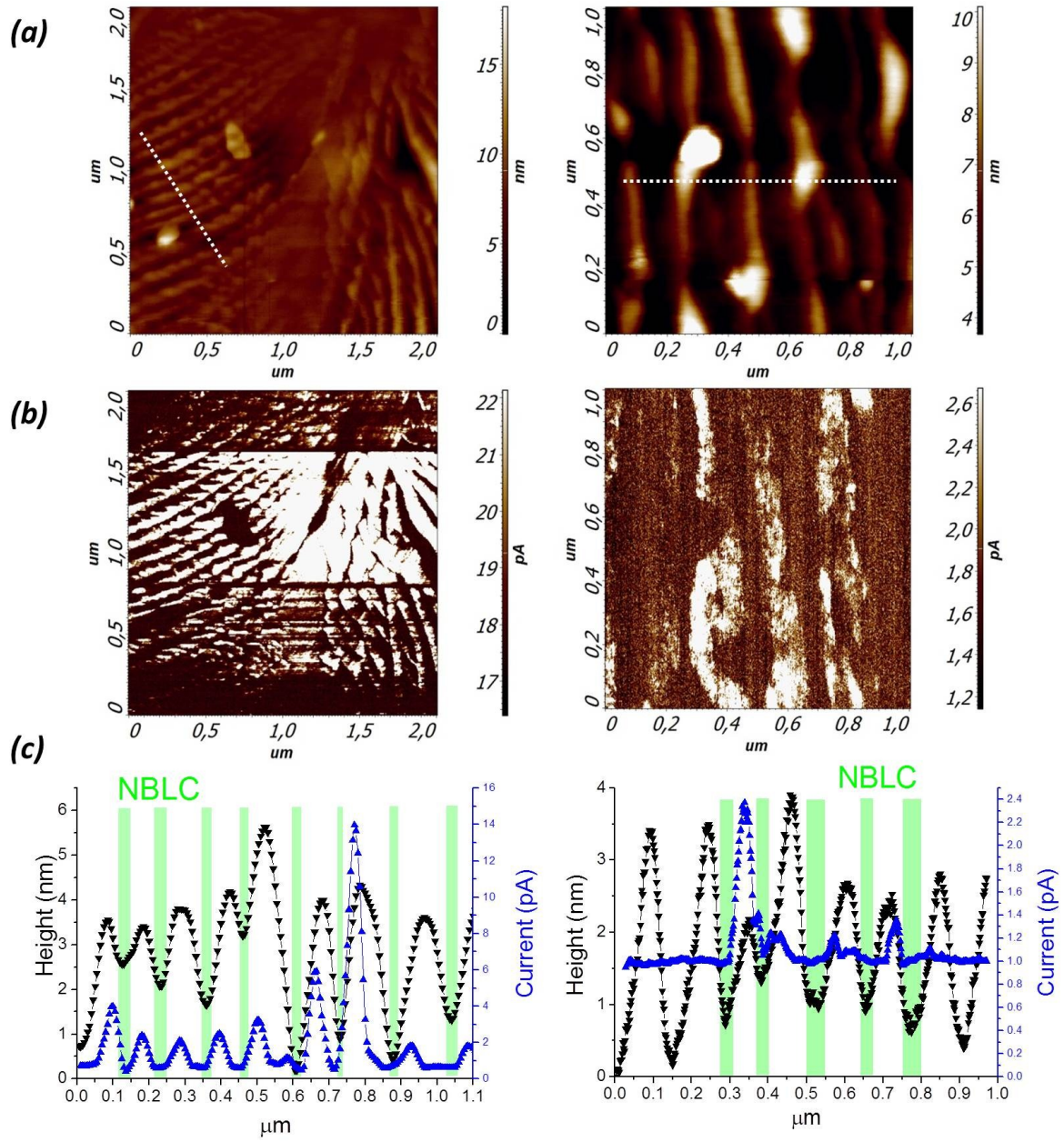


Figure 5. Topography (a), corresponding current distribution (b) and their profiles (c) obtained for the terrace ledge 1 (left) and terrace ledge 2 (right) domain areas.

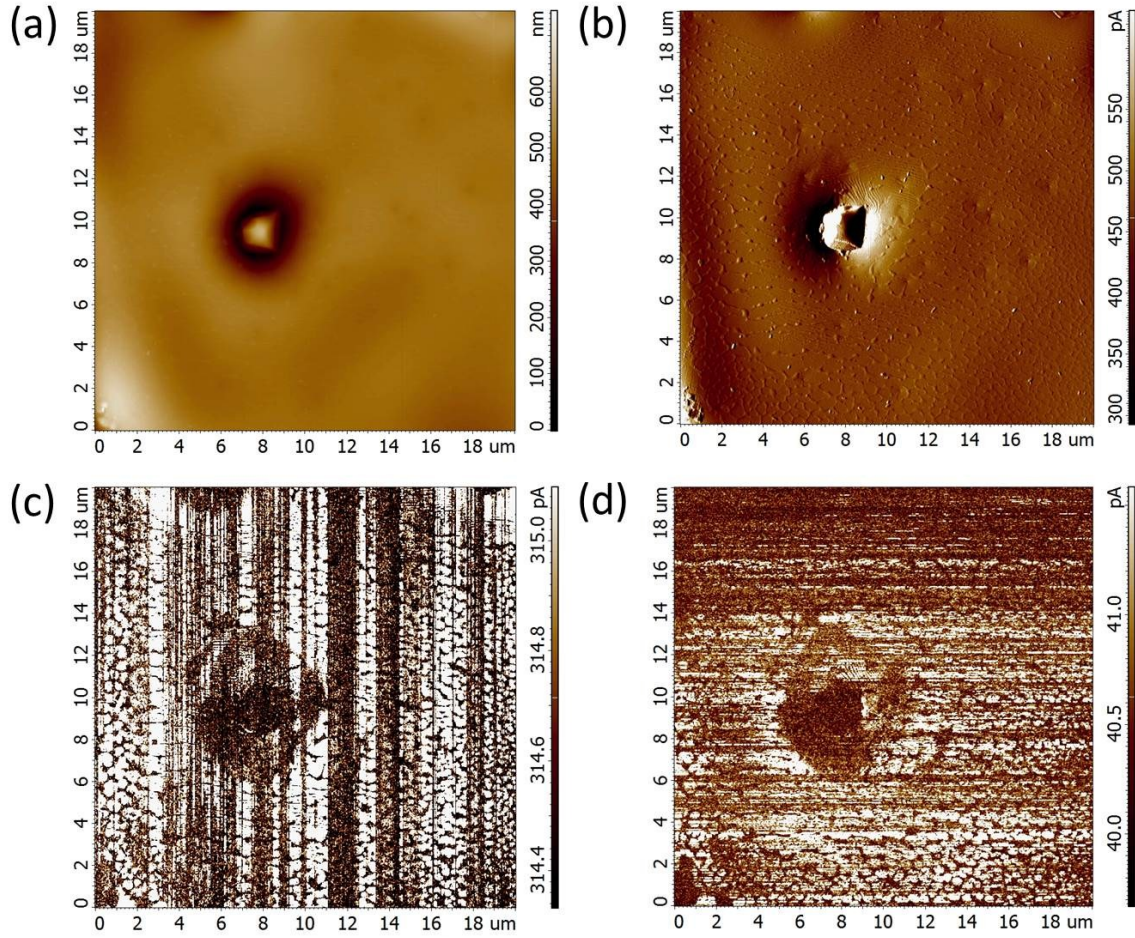


Figure 6. Topography (a), DFL response (b) and corresponding top-to-down (c) and left-to-right (d) SR scans. The scan was done at 0.3 Hz (512 x 512 pixels) and dc bias voltage of 1 V.

References

1. T. Fang and H.-K. Shiao, Mechanism for Developing the Boundary Barrier Layers of $\text{CaCu}_3\text{Ti}_4\text{O}_{12}$, J. Am. Ceram. Soc. 87 (2004) 2072-2079.