Electronic Supplementary Material (ESI) for RSC Advances.

N-channel and P-channel Few-layer InSe Photoelectric Devices

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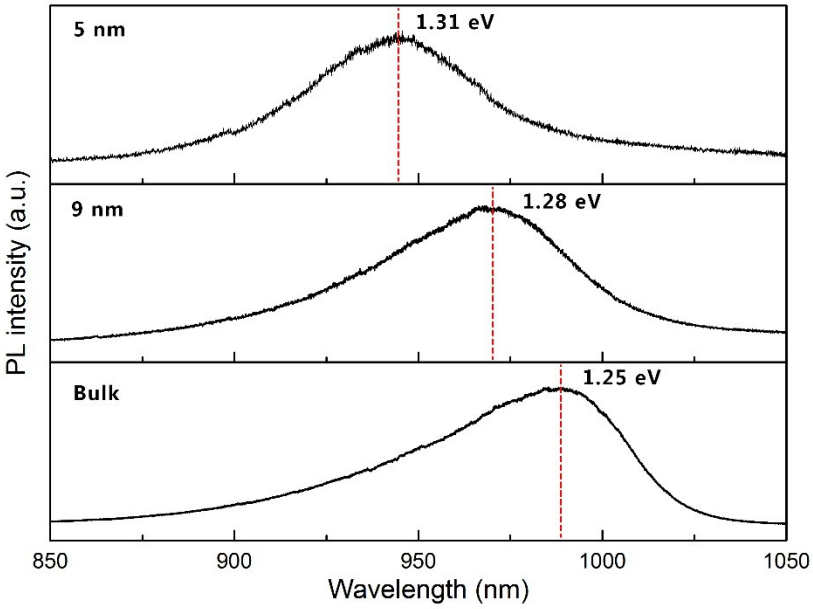

Figure S1. PL spectra InSe sheets with thickness of 5 nm, 9 nm and bulk, indicating a direct band gap of 1.31 eV, 1.28 eV and 1.25 eV, respectively.

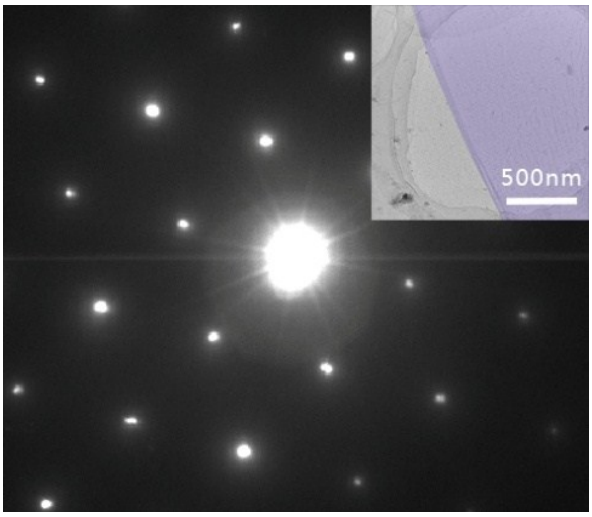

Figure S2. Selected area electron diffraction pattern of the InSe nanosheet, displaying typical six-fold symmetry in its [001] lattice plane. The light blue area in the inset was the few-layer InSe nanosheet being transferred onto Cu grid.

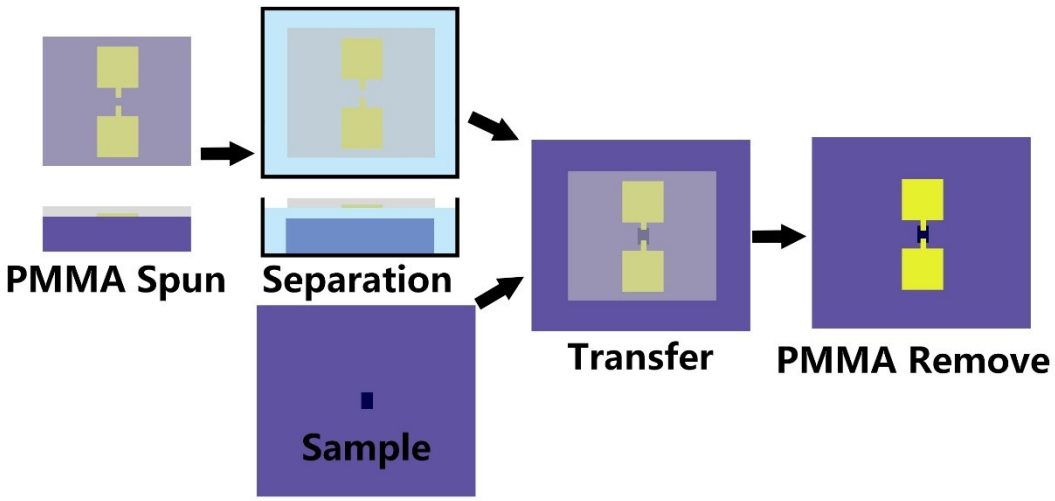

Figure S3. Schematic of the photolithographic-pattern transfer technique for fabricating back gate InSe FET devices. And the detailed process can be seen below. 8% PMMA in monochlorotoluene was spun onto the SiO2/Si chips with gold electrode patterns on at 2000 rpm and then baked on a 150 °C heating plate for 1 h. After that, chips were immersed in 50 °C NaOH solution for 30 min to separate the PMMA with electrode arrays from substrate. Then, the PMMA film was transferred onto the sample on another substrate, and the electrodes and sample aligned manually with the help of microscope. Finally, the dry PMMA

film was dissolved in acetone and the device was completed. The whole process can also be seen in (Advanced Materials Technologies, 2016, 1(1)).