

## Supporting Information

# Tunable graphene doping by modulating nanopores geometry on SiO<sub>2</sub>/Si substrate

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## **S1. Details of the substrate-cleaning and the CVD graphene transfer processes**

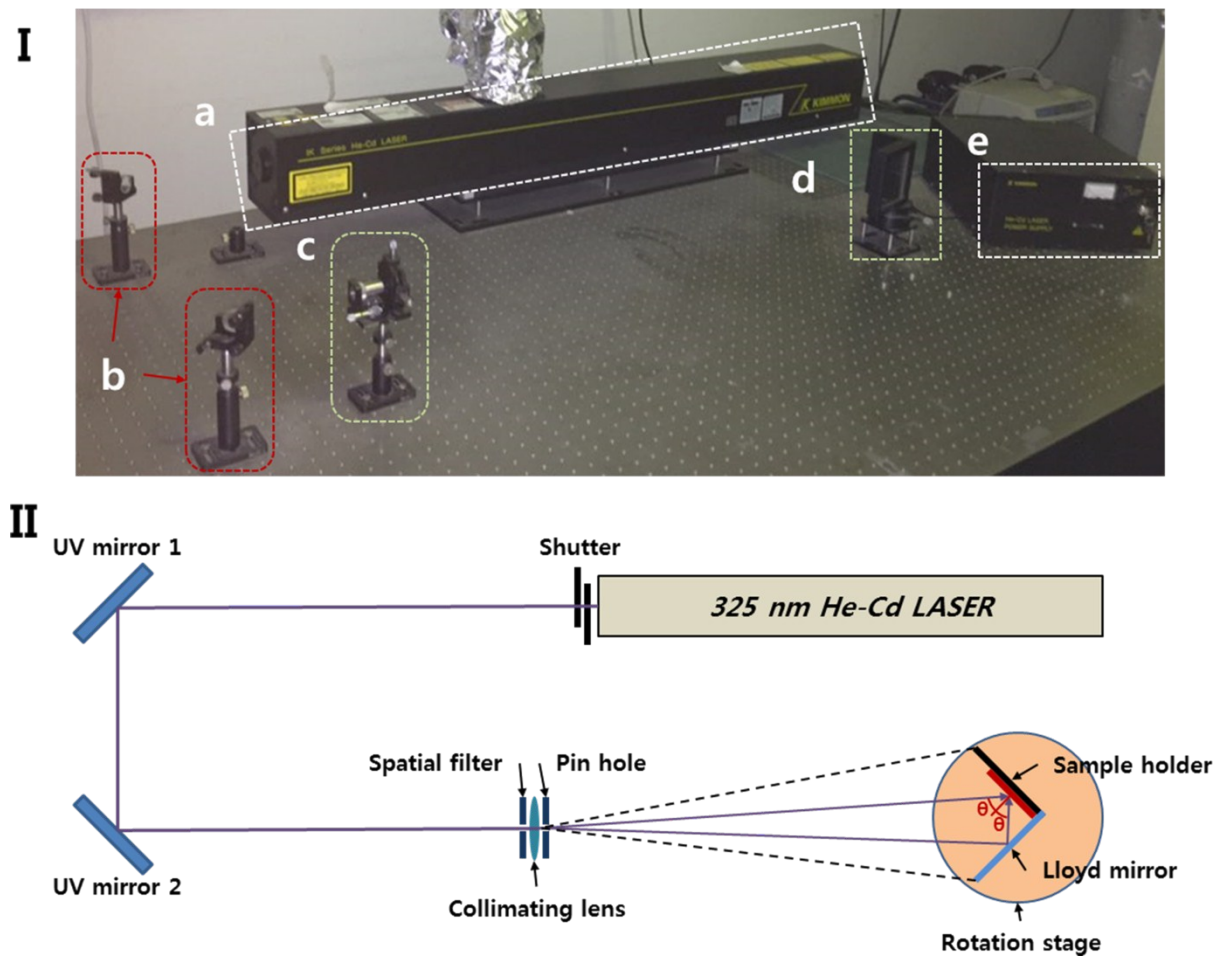
### **I. Substrate-cleaning process**

1. Sonication of the prepared substrates with acetone, methanol and DI water in order for 5 min., respectively.
2. SC-1 treatment (SC-1 solution;  $\text{NH}_4\text{OH} : \text{H}_2\text{O}_2 : \text{H}_2\text{O} = 1:1:5$ ) for 10 min (80 °C).
3. Rinse with DI water for 5 min.

### **II. CVD graphene transfer process**

1. PMMA (PMMA A4, MicroChem) spin-coating onto graphene/Cu foil with 3000 RPM.
2. Baking the sample on the hot-plate at 80 °C.
3. Etch the Cu-foil in Cu-etchant (CE-100, transgene, Company, Inc.).
4. Rinse twice with DI water for 5 min., respectively.
5. Cleaning with 5 % HCl aqueous solution to remove the contaminants generated during Cu etching process.
6. Again, rinse twice with DI water for 5 min., respectively.
7. Transfer the PMMA/graphene onto the prepared substrates and dry under  $\text{N}_2$  ambient (10 h).
8. Baking PMMA/graphene/substrate sample on the hot plate (150 °C) for 10 min.
9. Remove PMMA by immersing in acetone for 1h (80 °C).
10. Take the sample out of the acetone, and dry with  $\text{N}_2$  blowing.
11. Vacuum annealing for 1 h (300 °C,  $1.6 \times 10^{-6}$  torr).

## S2. Laser interference lithography (LIL) system



**Fig. S2. I.** Actual image of the laser interference lithography (LIL) system used in this research: **a.** He-Cd laser ( $\lambda = 325$  nm), **b.** UV mirrors, **c.** spatial filter - collimating lens - pin hole set, **d.** rotating stage, and **e.** power supply. **II.** Schematic of the LIL system.

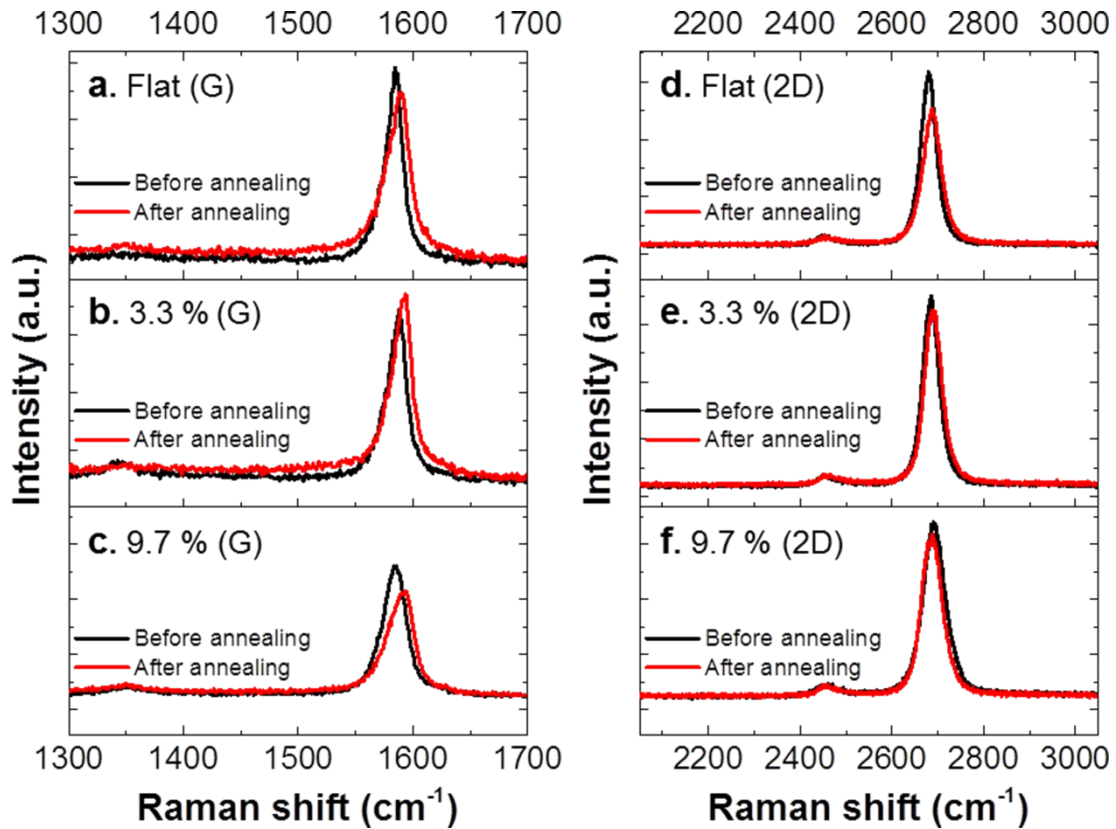
The 325 nm UV-laser beam was generated by the He-Cd laser system and was reflected by two successive identical UV mirrors to change its direction into the spatial filter. By passing through the spatial filter, the UV-laser beam was enhanced by diffraction. Then, the enhanced beam was illuminated onto the rotation stage in which the sample holder and the Lloyd mirror were vertically located. During the illumination, the direct beam and the beam

reflected from the Lloyd mirror were interfered to generate the periodic line beam intensity. By controlling the Lloyd mirror angle, the periodicity of the beam intensity can be tuned as follows;

$$\lambda = \frac{\lambda_{UV}}{2 \sin\theta}$$

Here,  $\lambda$ ,  $\lambda_{UV}$ , and  $\theta$  are the pitch size, the wave length of the UV laser (325 nm), and the incident angle, respectively. By utilizing this system, the periodic line patterns can be easily fabricated in a relatively large area ( $\sim 1 \text{ cm}^2$ ). The hole array can also be produced by double exposure with the sample rotated by 90 degrees and half of the total dose in each exposure.

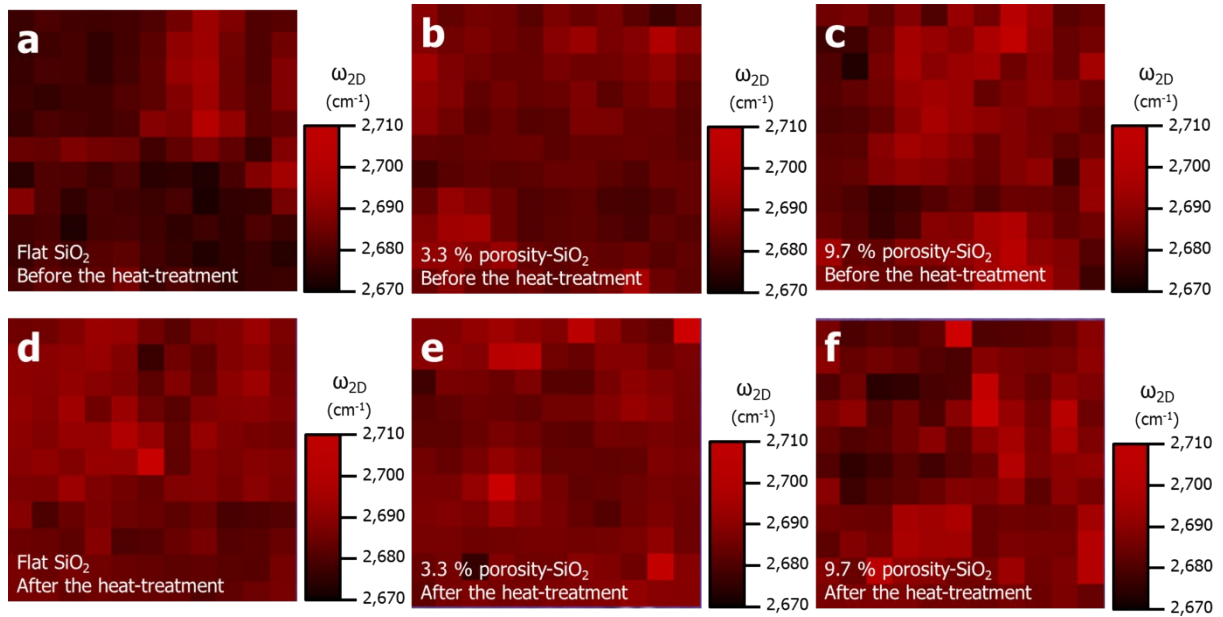
### “S3. Comparison of Raman spectra before and after annealing process



**Fig. S3.** Raman G- and 2D-peak shifts of graphene transferred on the substrates after annealing process ((a) and (d); flat SiO<sub>2</sub>, (b) and (e); 3.3 % porosity SiO<sub>2</sub>, (c) and (f); 9.7 % porosity SiO<sub>2</sub>)

It is reported that both the G- and 2D-peaks were red-shifted after heat-treatment, implying that tensile strain switched to compressive strain (*Nat. Commun.*, 2012, **3**, 1024). In our results, all the G-peaks (shown in (a), (b) and (c)) were red-shifted, which is consistent with the results of the reference. On the other hand, the 2D-peaks were slightly red-shifted except for the case of 9.7 %.

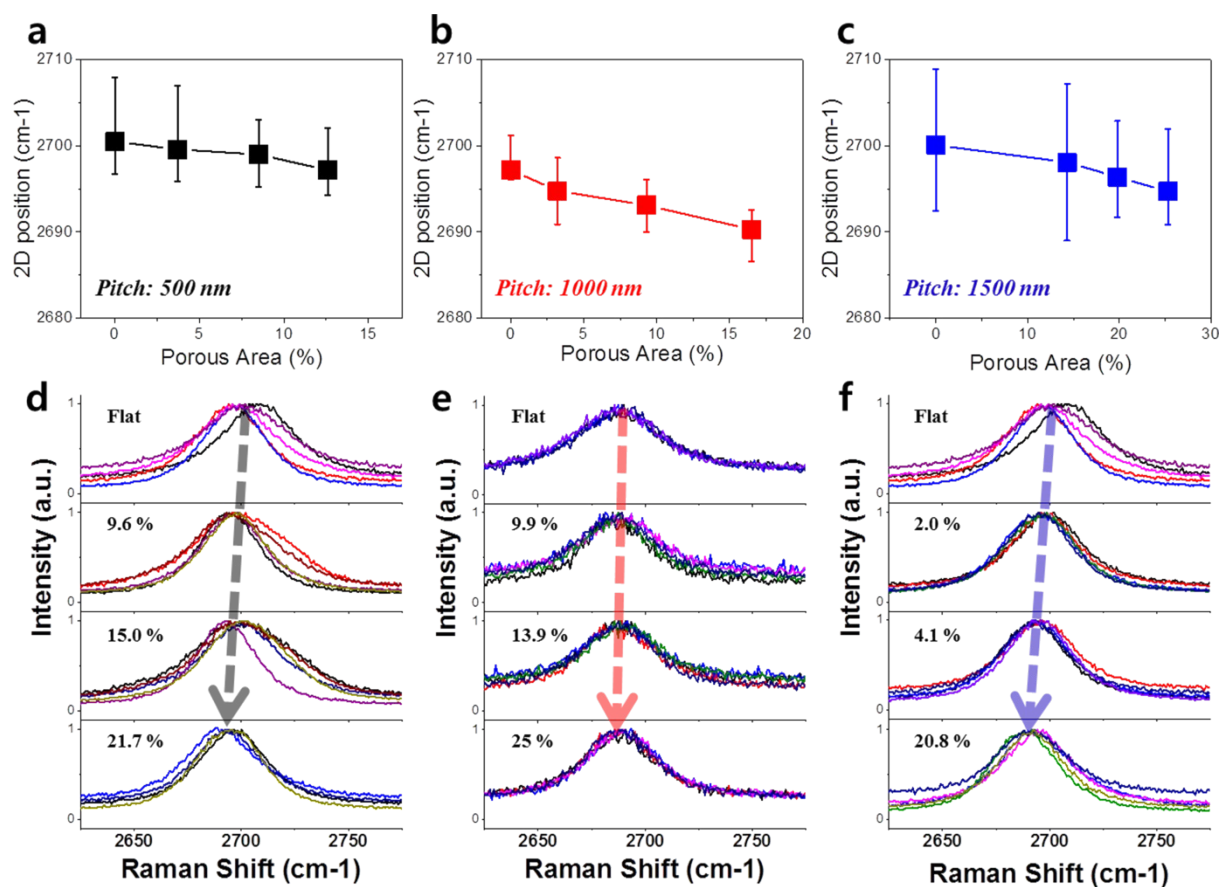
#### S4. Raman 2D-peaks mapping before and after annealing process



**Fig. S4.** Raman spectra were measured with 1  $\mu\text{m}$  step in  $10 \times 10 \mu\text{m}^2$  area and 2D-peaks of graphene were mapped in each substrate (flat and NP substrates with 3.3 % and 9.7 % porosities); (a), (b), and (c); before heat treatment. (d), (e), and (f); after heat treatment at 300  $^{\circ}\text{C}$ .

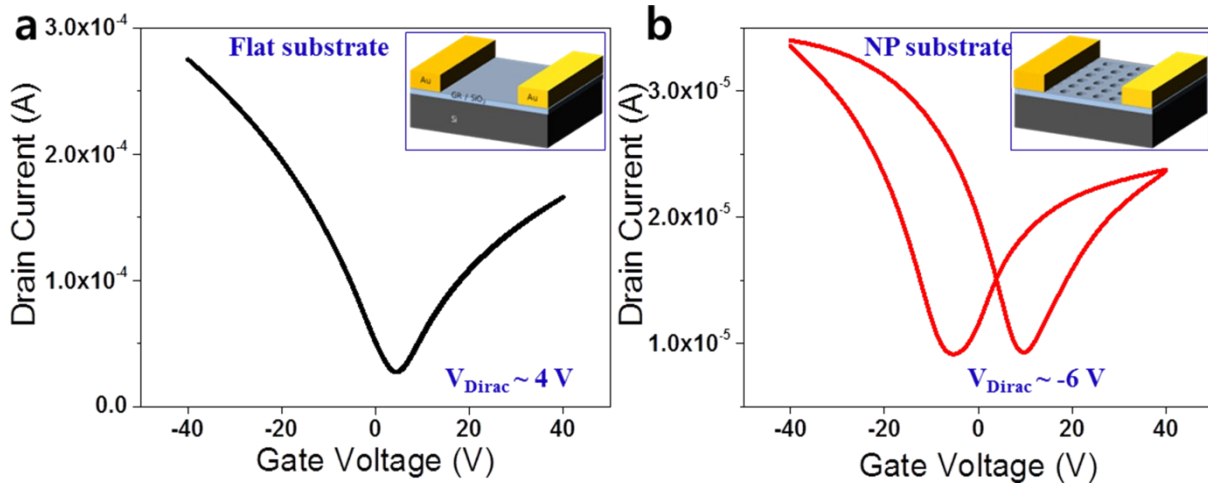
It is known that 2D-peak of graphene is red-shifted after annealing process (*Nat. Commun.*, 2012, **3**, 1024). In the case of flat  $\text{SiO}_2$  substrate (Fig. S5a and d), the color change is obvious. However, in the case of the NP substrates (Fig. S5b and e for 3.3 %, and Fig. S5c and f for 9.7 % porosity substrate), the color change is minimal, indicating that less compressive strain was occurred to the suspended graphene on the nanopores during the heat treatment.

**S5. Blue-shift of the 2D peak in Raman spectra with increasing porosity at different pitches**



**Fig. S5.** Blue-shift of the 2D peak in Raman spectra with increasing porosity, indicating the relative  $n$ -doping of the transferred graphene on the NP SiO<sub>2</sub>/Si substrate at different pitches of (a) 500 nm, (b) 1000 nm, and (c) 1500 nm. The corresponding Raman spectra of (d), (e), and (f) demonstrate the magnified 2D peaks from 5 points in each sample, showing the blue-shift of the 2D peak. As the porosity increased, the degree of blue-shift gradually increased in all cases. All the samples having the same pitch were fabricated together in the same conditions.

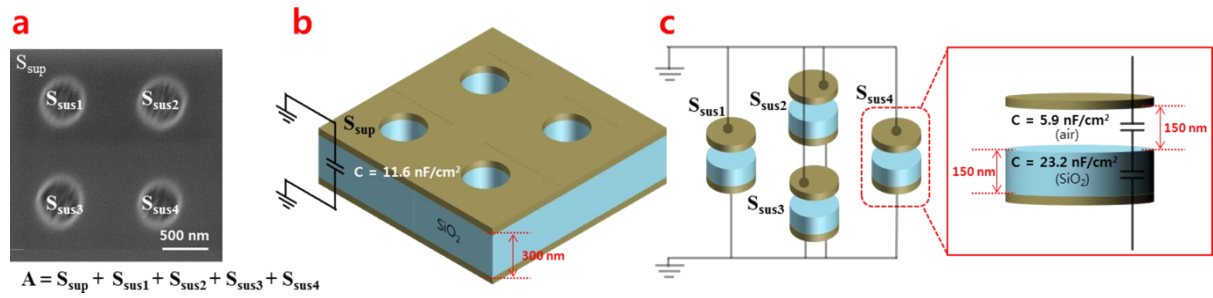
**S6. Current-level comparison of the  $I_D$ - $V_G$  curves from the top-contact G-FETs; flat substrate vs. NP substrate**



**Fig. S6.** Transfer curves ( $V_G$ - $I_D$ ) of the top-contact G-FETs fabricated on the (a) flat and (b) NP SiO<sub>2</sub>/Si substrates; inset shows the respective schematic top-contact G-FET image. The drain current ( $I_D$ ) level of the G-FET on the NP SiO<sub>2</sub>/Si substrate was one order of magnitude lower than that on the flat SiO<sub>2</sub>/Si substrate. The flat substrate device showed minimal hysteresis compared to the large hysteresis from the NP substrate device.



## S7. Calculation of the total capacitances of the NP SiO<sub>2</sub>/Si substrate



**Fig. S7.** (a) A SEM image of a NP SiO<sub>2</sub>/Si substrate; ‘S<sub>sup</sub>’ indicates the non-porous area that supports the transferred graphene, and ‘S<sub>sup1</sub>’ ~ ‘S<sub>sup4</sub>’ indicate the area of each nanopore, on which the transferred graphene is suspended. Actually, a tremendous number of nanopores exist in the active channel area. In this figure, for simplicity, only four nanopores are illustrated. ‘A’ is the total active channel area expressed by (A = S<sub>sup</sub> + S<sub>sus1</sub> + S<sub>sus2</sub> + S<sub>sus3</sub> + S<sub>sus4</sub> + ...). When a graphene layer is transferred onto the NP SiO<sub>2</sub>/Si substrate, two kinds of capacitances can be considered; one is the (b) 300 nm-thick SiO<sub>2</sub> capacitance in the area of supported graphene (C = 11.6 nF/cm<sup>2</sup>) and the other is the (c) serially connected 150 nm-thick SiO<sub>2</sub> (23.2 nF/cm<sup>2</sup>) and 150 nm-thick air (5.9 nF/cm<sup>2</sup>) capacitances in the area of the suspended graphene (nanopore area).

The capacitance of the serially connected two capacitances within each nanopore (red dotted rectangular area in Figure S4c) can be calculated per cm<sup>2</sup> using Eq. S1;

$$\frac{1}{C_{nanopore}} = \frac{1}{C_{150\text{ nm thick air}}} + \frac{1}{C_{150\text{ nm thick SiO}_2}} \quad Eq. S1$$

$$1/C_{nanopore} = 1/5.9 + 1/23.2 = 0.212$$

$$\therefore C_{nanopore} = 4.36 \text{ [nF/cm}^2\text{]}$$

In the case of (c), a tremendous number of capacitors with the same structure are connected in parallel. Thus, the capacitance of total nanopores can be the sum of each nanopore capacitance using Eq. S2;

$$C_{total\ nanopores} = C_1 + C_2 + C_3 + C_4 + \dots \quad Eq. S2$$

$$C_{total\ nanopores} = 4.36 \text{ nF/cm}^2 \times (S_{sus1} + S_{sus2} + S_{sus3} + S_{sus4} + \dots) / A$$

$$C_{total\ nanopores} = 4.36 \text{ nF/cm}^2 \times \text{porosity [\%]}$$

Finally, overall capacitance is the combination of capacitance (b) and (c) in parallel, which can be simply calculated by adding the two types of capacitances (per unit area of  $\text{cm}^2$ ) multiplied by their respective area fractions using Eq. S3;

$$C_{\text{overall}} = 11.6 [\text{nF}/\text{cm}^2] \times (1 - \text{porosity}) + 4.36 [\text{nF}/\text{cm}^2] \times \text{porosity} \quad \text{Eq. S3}$$

Using Eq. S3, the overall capacitances of various dielectric layers with different porosities can be calculated as following;

### 1. Pitch: 1500 nm

i) *When the porosity is 9.6 %,*

$$C_{\text{overall}} = C_{\text{support}} + C_{\text{suspended}} = 11.6 [\text{nF}/\text{cm}^2] \times 0.904 + 4.36 [\text{nF}/\text{cm}^2] \times 0.096 = 10.94 [\text{nF}/\text{cm}^2]$$

ii) *When the porosity is 15.0 %,*

$$C_{\text{overall}} = 11.6 [\text{nF}/\text{cm}^2] \times 0.85 + 4.36 [\text{nF}/\text{cm}^2] \times 0.15 = 10.57 [\text{nF}/\text{cm}^2]$$

iii) *When the porosity is 21.7 %,*

$$C_{\text{overall}} = 11.6 [\text{nF}/\text{cm}^2] \times 0.783 + 4.36 [\text{nF}/\text{cm}^2] \times 0.217 = 10.11 [\text{nF}/\text{cm}^2]$$

### 2. Pitch: 1000 nm

i) *When the porosity is 9.9 %,*

$$C_{\text{overall}} = 11.6 [\text{nF}/\text{cm}^2] \times 0.901 + 4.36 [\text{nF}/\text{cm}^2] \times 0.099 = 10.92 [\text{nF}/\text{cm}^2]$$

ii) *When the porosity is 13.9 %,*

$$C_{\text{overall}} = 11.6 [\text{nF}/\text{cm}^2] \times 0.861 + 4.36 [\text{nF}/\text{cm}^2] \times 0.139 = 10.65 [\text{nF}/\text{cm}^2]$$

iii) *When the porosity is 25 %,*

$$C_{\text{overall}} = 11.6 [\text{nF}/\text{cm}^2] \times 0.861 + 4.36 [\text{nF}/\text{cm}^2] \times 0.139 = 9.89 [\text{nF}/\text{cm}^2]$$

### 3. Pitch: 500 nm

i) *When the porosity is 2.0 %,*

$$C_{\text{overall}} = 11.6 [\text{nF}/\text{cm}^2] \times 0.98 + 4.36 [\text{nF}/\text{cm}^2] \times 0.02 = 11.46 [\text{nF}/\text{cm}^2]$$

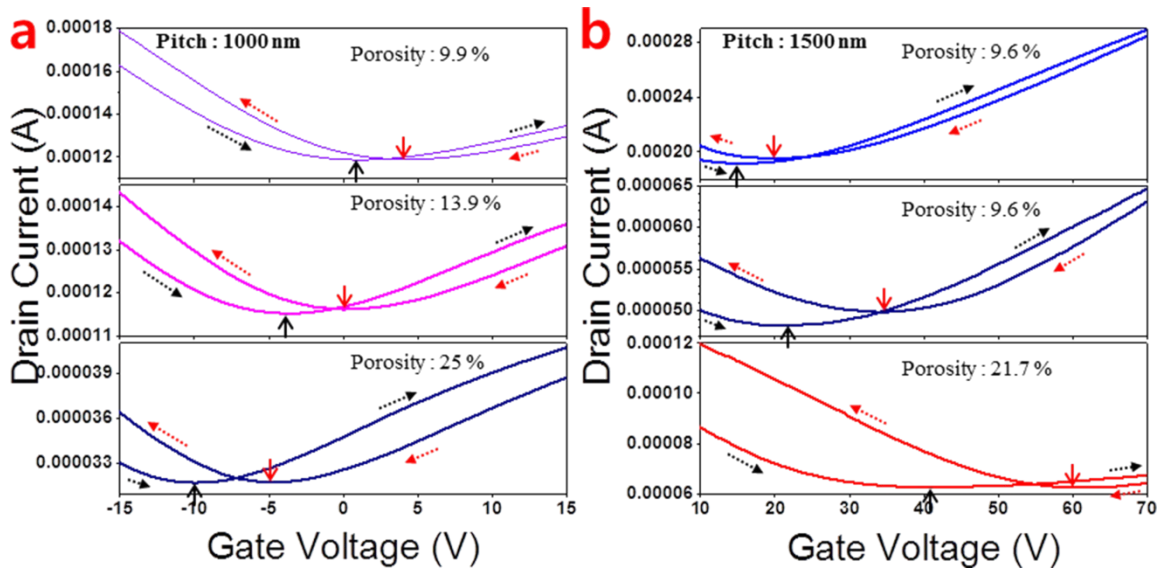
ii) *When the porosity is 4.1 %,*

$$C_{\text{overall}} = 11.6 [\text{nF}/\text{cm}^2] \times 0.959 + 4.36 [\text{nF}/\text{cm}^2] \times 0.041 = 11.32 [\text{nF}/\text{cm}^2]$$

iii) *When the porosity is 20.8 %,*

$$C_{\text{overall}} = 11.6 [\text{nF}/\text{cm}^2] \times 0.792 + 4.36 [\text{nF}/\text{cm}^2] \times 0.208 = 10.17 [\text{nF}/\text{cm}^2]$$

### S8. Dirac voltage shift of the transfer curves



**Fig. S8.** Dirac voltage shift and hysteresis of the transfer curves during the dual-sweep from -50 V to +50 V (zoomed in around the Dirac voltage) for the G-FETs on the NP substrate at a pitch of (a) 1000 nm and (b) 1500 nm. The arrows indicate the Dirac voltages during forward (black) and backward (red) sweeps.