

Electronic Supplemental Information

Highly-ordered silicon nanowire arrays for photoelectrochemical hydrogen evolution: An investigation on the effect of wire diameter, length and inter-wire spacing

Sitaramanjaneya Mouli Thalluri,^a Jerome Borme,^a Dehua Xiong,^a Junyuan Xu,^a Wei Li,^a Isilda Amorim,^a Pedro Alpuim,^{a,b} Joao Gaspar,^a Helder Fonseca,^a Liang Qiao^c and Lifeng Liu^{a,*}

^a *International Iberian Nanotechnology Laboratory (INL), Av. Mestre Jose Veiga, 4715-330 Braga, Portugal*

^b *CFUM-Center of Physics of the University of Minho, 4710-057, Braga, Portugal*

^c *Department of Chemistry, Fudan University, 200433 Shanghai, China*

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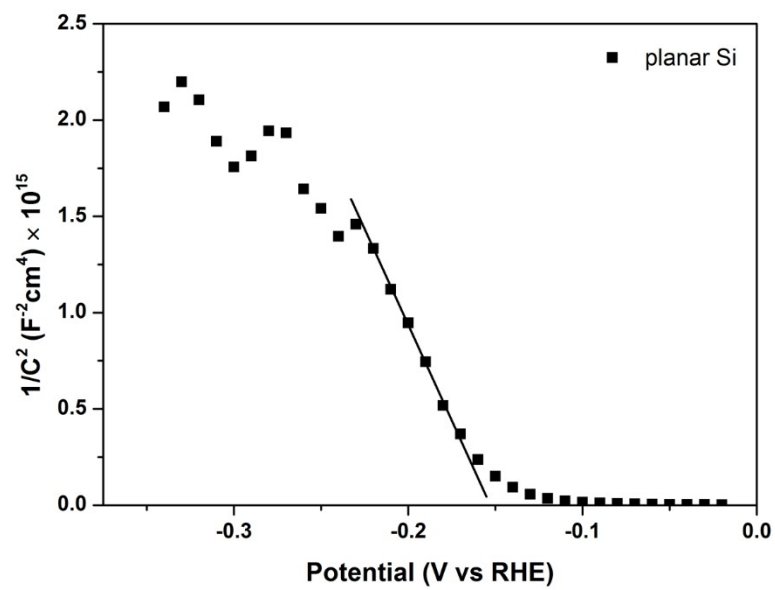


Fig. S1 Mott-Schottky plot of the planar Si substrate.

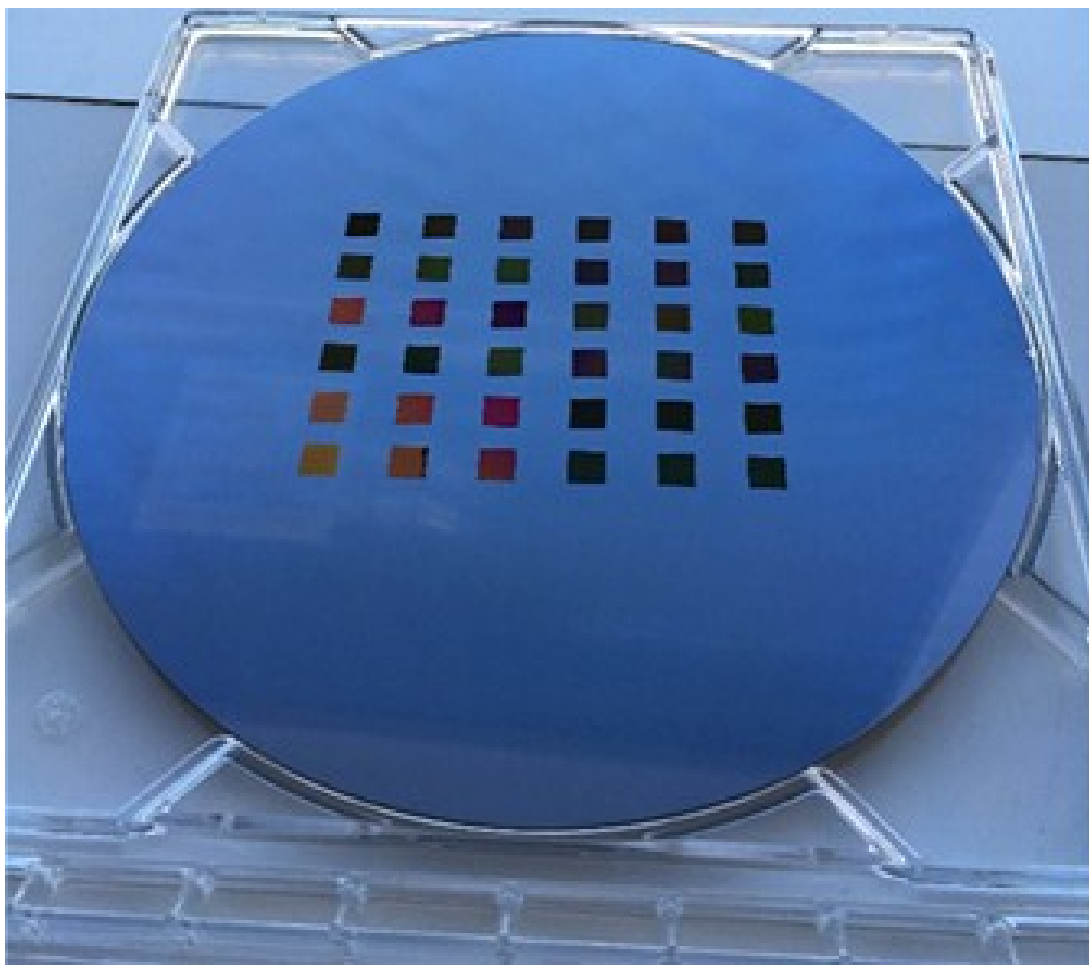


Fig. S2 Digital photograph showing the fabrication of SiNW arrays on a large scale ($36 \times 0.5 \text{ cm}^2$ patterned areas) over a 200 mm p-Si wafer employing e-beam lithography and subsequent DRIE process.

E-beam lithography process:

Negative tone resist AR-N 7520.18 old (Allresist, Germany) was diluted with thinner AR 300.12 (1:1) and then used as the photoresist for e-beam lithography. The solution was spin-coated on a Si wafer at 2750 rpm and baked at 85 °C for 60 s, forming a layer of 200 nm. The electron exposure (Vistec EBPG 5200) was performed at 100 kV of acceleration voltage with a dose $1100 \mu\text{C cm}^{-2}$. The features exposed were squares of the nominal size chosen, but the etching process rounds the corners of the features. The choice of square features rather than circular one allows for a much faster electron beam exposure due to the simpler trapezoid decomposition of square features.

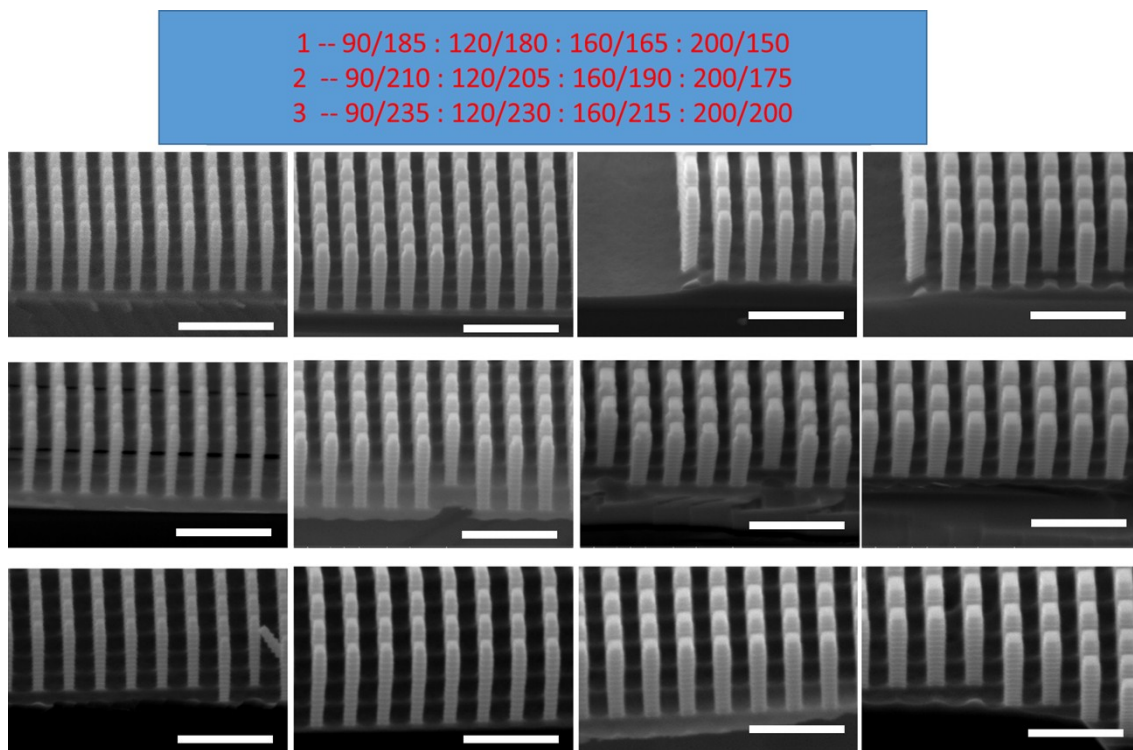


Fig. S3 SEM images showing the morphology of highly-ordered SiNW arrays with different combinations of wire diameter and inter-wire spacing. Scale bars: 1 μm . The numbers above the images refer to the measured wire diameters and inter-wire spacing.

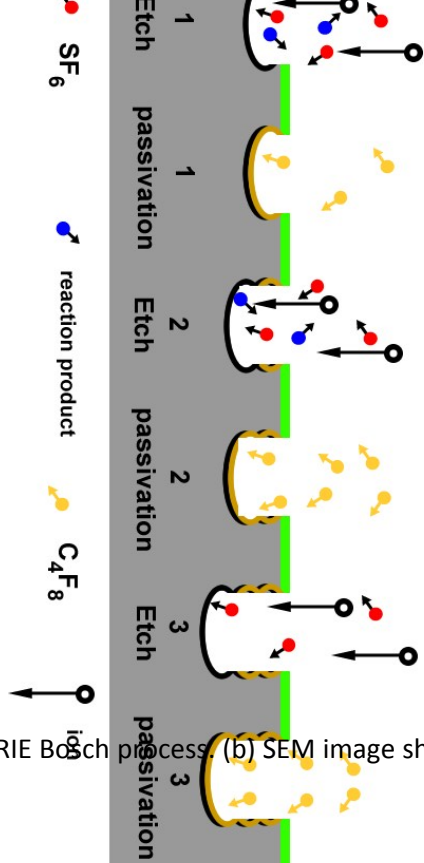
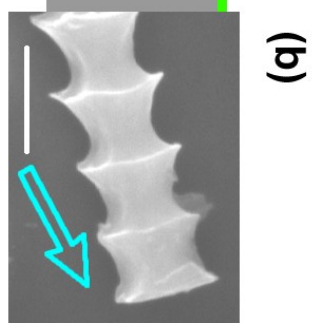


Fig. S4 (a) Schematic illustration of the DRIE Bosch process. (b) SEM image showing a resulting individual NW. Scale bar: 100 nm.



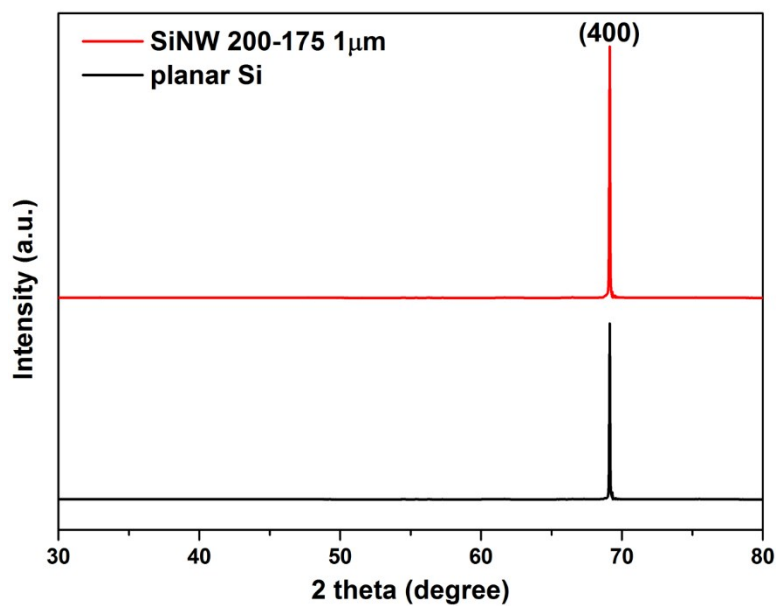


Fig. S5 XRD patterns of planar Si and SiNW 200-175 1 μ m, which illustrates that the crystal structure of Si was not altered by the e-beam lithography and subsequent DRIE process. The diffraction peaks are indexed in accordance with the standard powder diffraction pattern of Si (JCPDS: 00-027-1402).

Table S1. Fitting parameters obtained by fitting the Nyquist plots presented in **Figure 4c** with the equivalent circuit models shown in the inset.

	R_s (Ω)	R_{ct} (Ω)	Q (μF)
Planar Si	6.4	75.4	8.1
SiNW 200-175 1 μm	6.2	7.4	90.3
SiNW 200-175 2 μm	10.3	12.3	41.0
SiNW 200-175 5 μm	7.6	26.5	31.6