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SUPPLEMENTARY INFORMATION

A Functional Micro-Solid Oxide Fuel Cell with Nanometer Freestanding Electrolyte

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Fabrication process for a micro-SOFC integrated with 10 nm-thick YSZ electrolyte

Figure S1(a) shows a schematic of fabrication process for 10 nm-thick freestanding YSZ electrolyte in detail. A four-inch (100) double-side polished silicon wafer with thickness of 400 μm was utilized as a supporting substrate. (a1) On top of the wafer, circular trenches were generated with photolithography and deep-reactive ion etching (DRIE). Circular trenches are arranged as a circular configuration in this work. The diameter of the circular trenches is 50 μm, and the etched depth is 30 μm. (a2) Low stress silicon nitride (Si_3N_4) layer with 200 nm in thickness was deposited as a passivation layer on both side of the wafer by low pressure chemical vapor deposition (LPCVD). Si_3N_4 on the backside was then patterned with square open windows for subsequent DRIE and KOH etching. Afterward, at the centers of the open windows, circular trenches were etched with the diameter that is 1 mm smaller than the lateral length of the square open window. (a3) Thin film YSZ electrolyte with thickness of 20 nm was deposited on wafer top side by atomic layer deposition (ALD) with conditions as found in [1, 2]. The deposited YSZ thin film conformally replicates the surface contour of pre-patterned circular trenches and forms a three-dimensional thin film. (a4) To further reduce the electrolyte thickness below 7-8 nm, oxide etching was performed by buffered oxide etchant (BOE, 10 % HF: H_2O) solution at room temperature. (a5) Additional YSZ deposition by ALD with thickness of 3~4 nm was then carried out on the etched YSZ surface. (a6) The silicon was etched by a through-wafer etching in 80 % KOH solution at 85 °C until 20 μm-thick silicon remained. During KOH etching, the YSZ layer was protected by an etching holder to avoid direct contact with KOH solution. After KOH etching, silicon-membrane supported micro-SOFC array templates were created and (a7) the Si_3N_4 layer underneath the YSZ layer was removed by reactive ion etching (RIE) with CF_4 and O_2 plasma. (a8) Lastly, nanoporous Pt electrodes of the micro-SOFC array were deposited on both sides by radio-frequency (RF) sputtering with conditions of 30 mTorr Ar base pressure and 100 W RF power at room temperature. After electrode deposition, all individual cells were connected in parallel and micro-SOFC arrays were placed on 10 mm × 10 mm diced silicon chips.

Figure S1(b) shows FESEM view of a dish-shaped and freestanding micro-SOFC with total thickness of 70 nm after completing fabrication process. Figure S1(c) shows FESEM bottom views of micro-SOFC array. Micro-SOFC cells were circularly arranged to form an array structure at the center of a silicon chip and each cell was supported by stress-free (100) silicon substrate. The periphery of the micro-SOFC array was fortified by a tapered structure which was evolved from the addition of the DRIE trench and the enhanced thermal mechanical stability of micro-SOFC array by an edge-reinforced structure was well discussed in our previous work.[3]

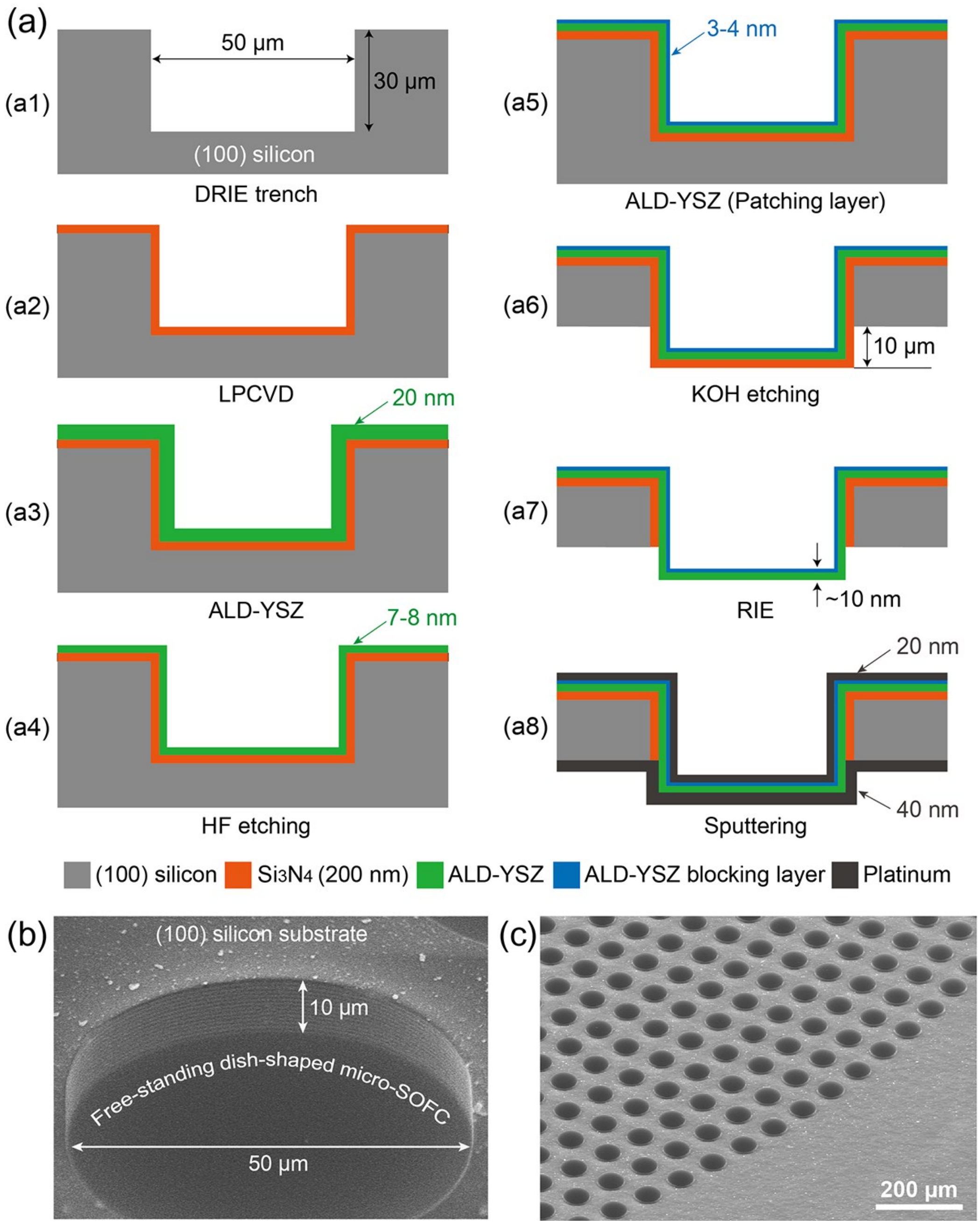

Figure S1. (a) Schematic of fabrication process for a micro-SOFC architecture featuring 10 nm-thick YSZ electrolytes. (b) FESEM view of a cell of micro-SOFCs after completing fabrication process. (c) FESEM bottom view of micro-SOFC array.

Survival rate comparison

To compare survival rates between 10 nm-thick single layer YSZ and bi-layer YSZ after fabrication process, total 32 cells were prepared respectively. Each cell is placed on a 10 mm ×10 mm diced silicon chip. Cell architecture and fabrication processes for other cell components were the same and membrane failure was confirmed by optical microscope.

All cells with 10 nm-thick single layer YSZ electrolyte were not survived after fabrication process and mostly broken during RIE etching process and sputtering process. However, 12 cells of total 32 cells with bi-layer YSZ electrolyte were survived during fabrication (survival rate: 37.5 %) and these cells were also survived during fuel cell operation.

References

(1) Su, P. C.; Chao, C. C.; Shim, J. H.; Fasching, R.; Prinz, F. B. *Nano Lett.* **2008,** 8, 2289-2292.

(2) Su, P. C.; Prinz, F. B. *Electrochem. Commun.* **2012,** 16, 77-79.

(3) Baek, J. D.; Yu, C.-C.; Su, P.-C. *Nano Lett.* **2016,** 16, 2413-2417.