Electronic Supplementary Material (ESI) for Journal of Materials Chemistry C.

Supporting Information

Vapor-phase synthesis of sub-15 nm hybrid gate dielectrics for organic thin film transistors

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Table S1 Comparison between ALD and iCVD process

		ALD	iCVD
Dimension & control of reactor	Shape of reactor	Disk	
	Height of reactor	1 ~ 3 cm	
	Flow delivery	By mass flow controller (MFC)	
Process condition	Initiation of reaction	By injecting reactant	By thermal initiation
	Process pressure	10 ~ 1000 mTorr	50 ~ 1000 mTorr
	Substrate temperature	60 ~ 400 °C	10 ~ 50 °C
	Deposition rate	0.5 ~ 1 nm/min	0.5 ~ 200 nm/min

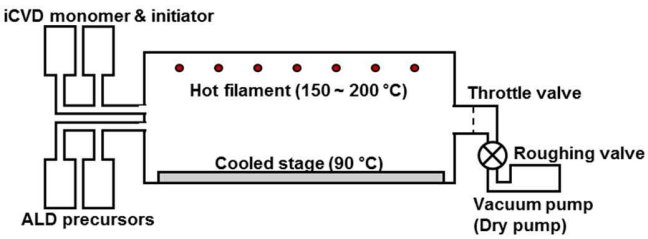

Fig. S1 Schematic of the single chamber system of ALD and iCVD.

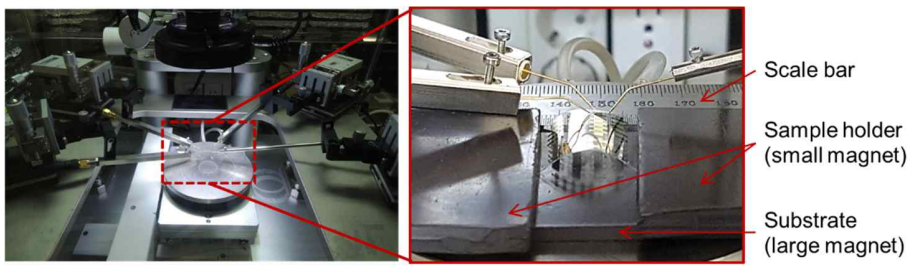

Fig. S2 Photograph of custom-built flexibility test equipment used in the manuscript.

Table S2 Optimized process condition for ALD and iCVD

	Process temperature (˚C)	Gas reaction time (s)	Gas purge time (s)	Deposition rate (nm/min)
Al_2O_3 ALD	90	5	15	0.60

	Process temperature (˚C)	Process pressure (mTorr)	Gas injection ratio (sccm : sccm)	Deposition rate (nm/min)
pV3D3 iCVD	40	300	2.5 : 1	1.0
	90	1500		0.8

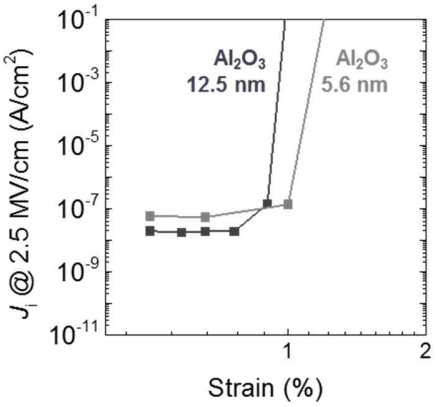

Fig. S3 Applied strain vs. J_i of MIM devices with ALD Al_2O_3 dielectric

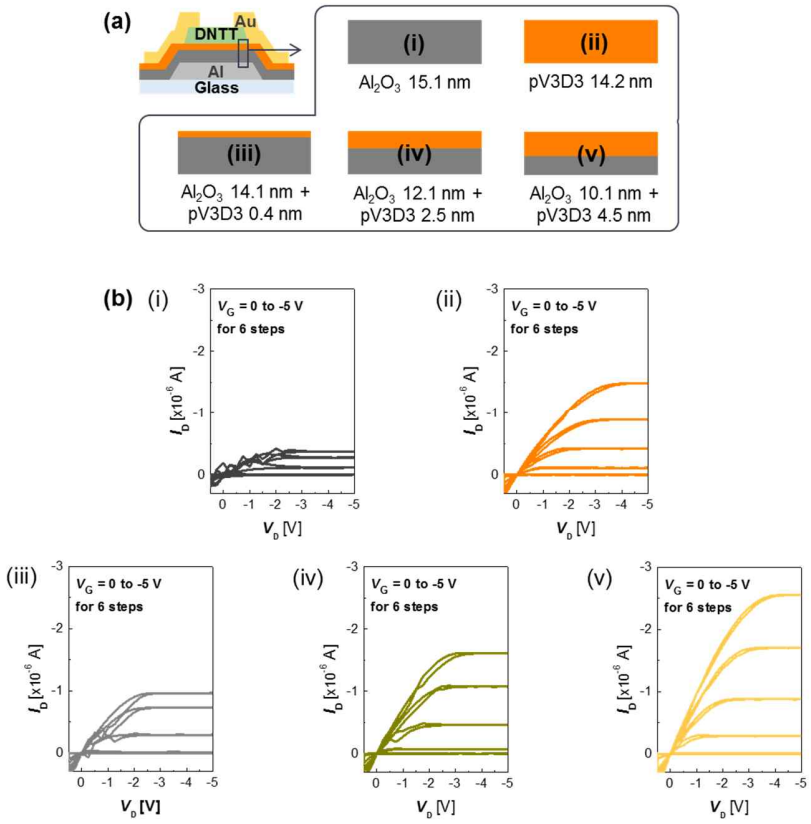

Fig. S4 (a) Device structure of DNTT TFTs fabricated in this work with different thickness compositions of dielectric layers: Single layer with (i) ALD Al_2O_3 and (ii) iCVD pV3D3, and (iii to v) hybrid layer with various thickness compositions. (b) Output characteristics of corresponding TFTs with dielectric layers from (i) to (v).

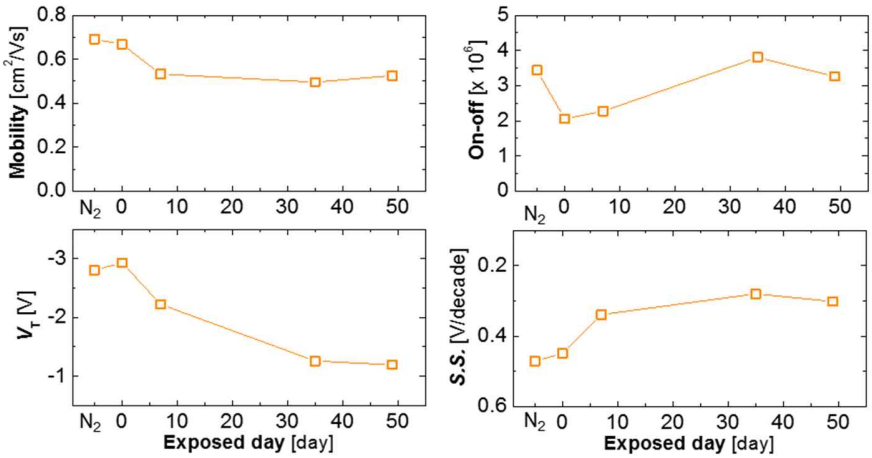

Fig. S5. Shelf-life stability of DNTT TFTs in ambient condition up to 49 days. C_i of device was 50 nF/cm^2 (39.0 nm of pV3D3 was used as a dielectric layer).

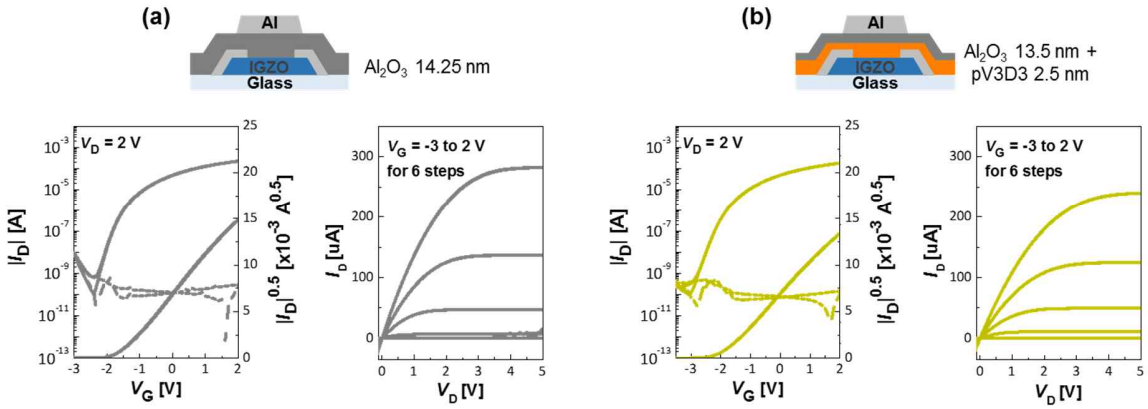

Fig. S6 Transfer and output characteristics of IGZO TFTs made with (a) ALD Al_2O_3 and (b) ALD Al_2O_3 and iCVD pV3D3 as dielectric layers, respectively.