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Supplementary Information

Real-time storage of thermal signal in organic memory with floating core-shell nanoparticles

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Experimental:

Preparation of Au nanoparticles

A 50 ml 1 mM $HAuCl_4 \cdot 3H_2O$ solution was brought to the boil, and then 5 ml of 37.8 mM sodium citrate was added to the boiling solution. Boiling was continued for another 20mins. The solution was left cool to room temperature.

Preparation of Pd nanoparticles

50 ml of 1mM aqueous Pd (II) salt solution was mixed with 50 ml of ethanol containing 1 ml of DDA. After 3 min of stirring, 50 ml of toluene was added, and stirring was continued for 1 min. Transfer metal ions from water to toluene. Then, at 100 °C, 1 ml of 100 mM of toluene solution of TBAB was added to 20 ml of the toluene solution of Pd (II) salt, and the mixture was agitated for 10 minutes.

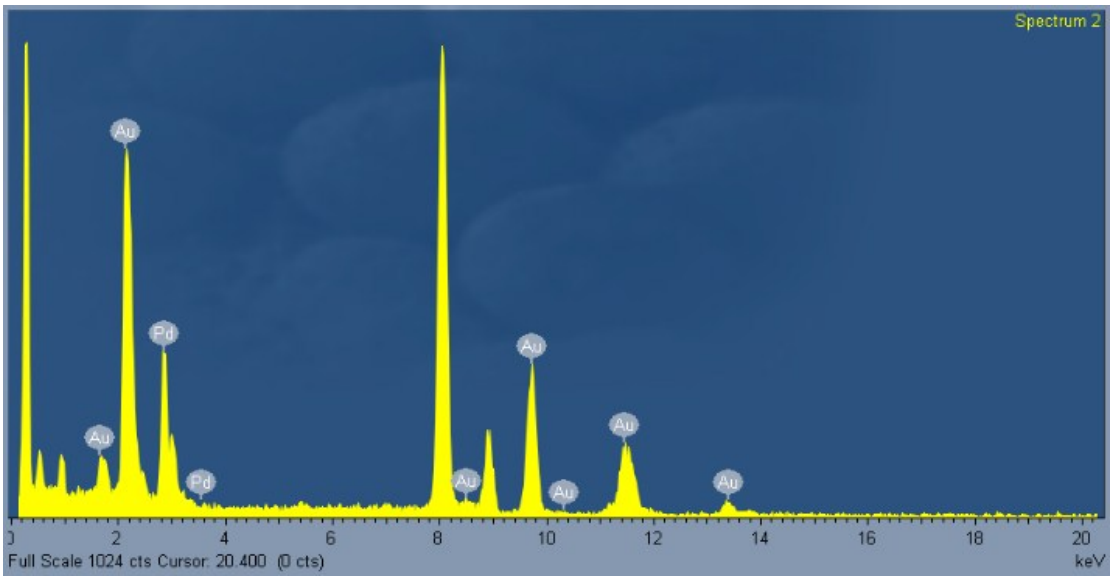

Fig. S1. EDS spectrum of the Au@Pd nanoparticle

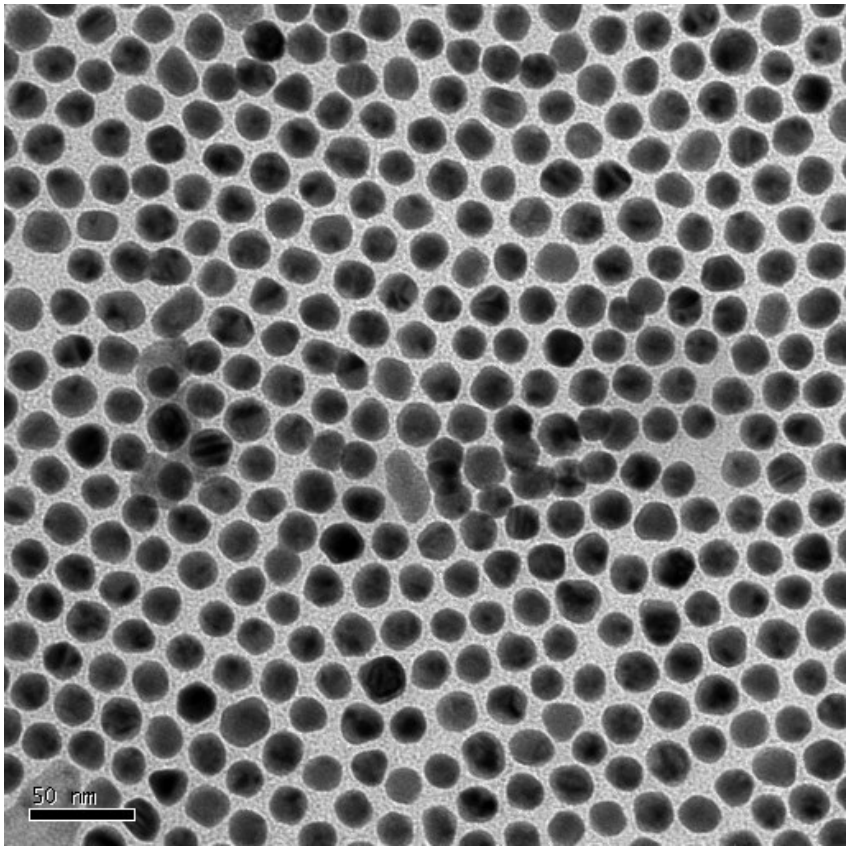

Fig. S2. TEM image of the fabricated Au@Pd nanoparticle monolayer.

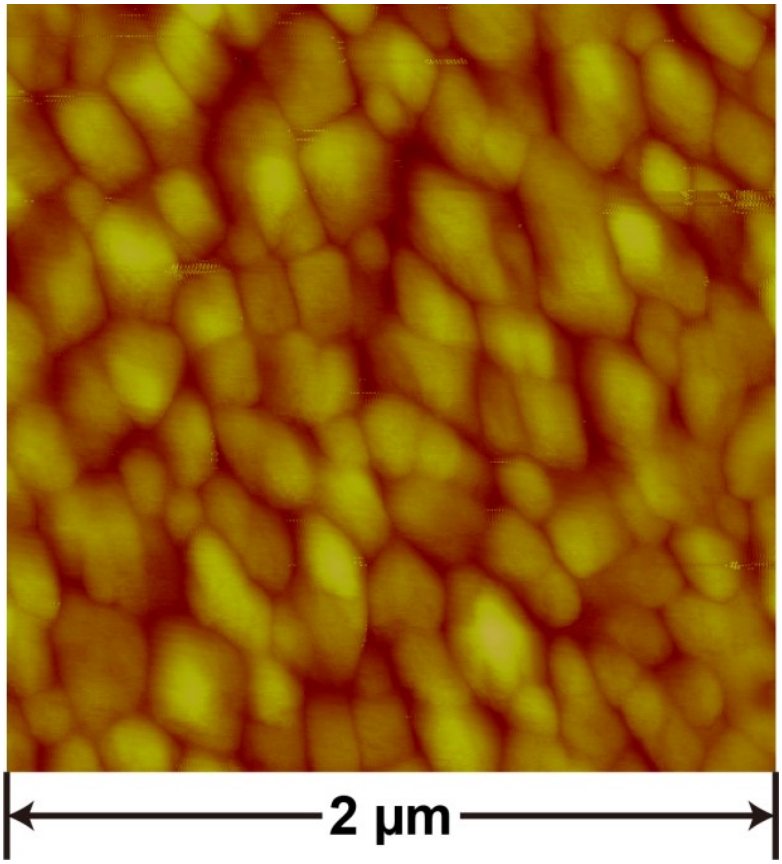

Fig. S3. AFM image of pentacene deposited on PET substrate.

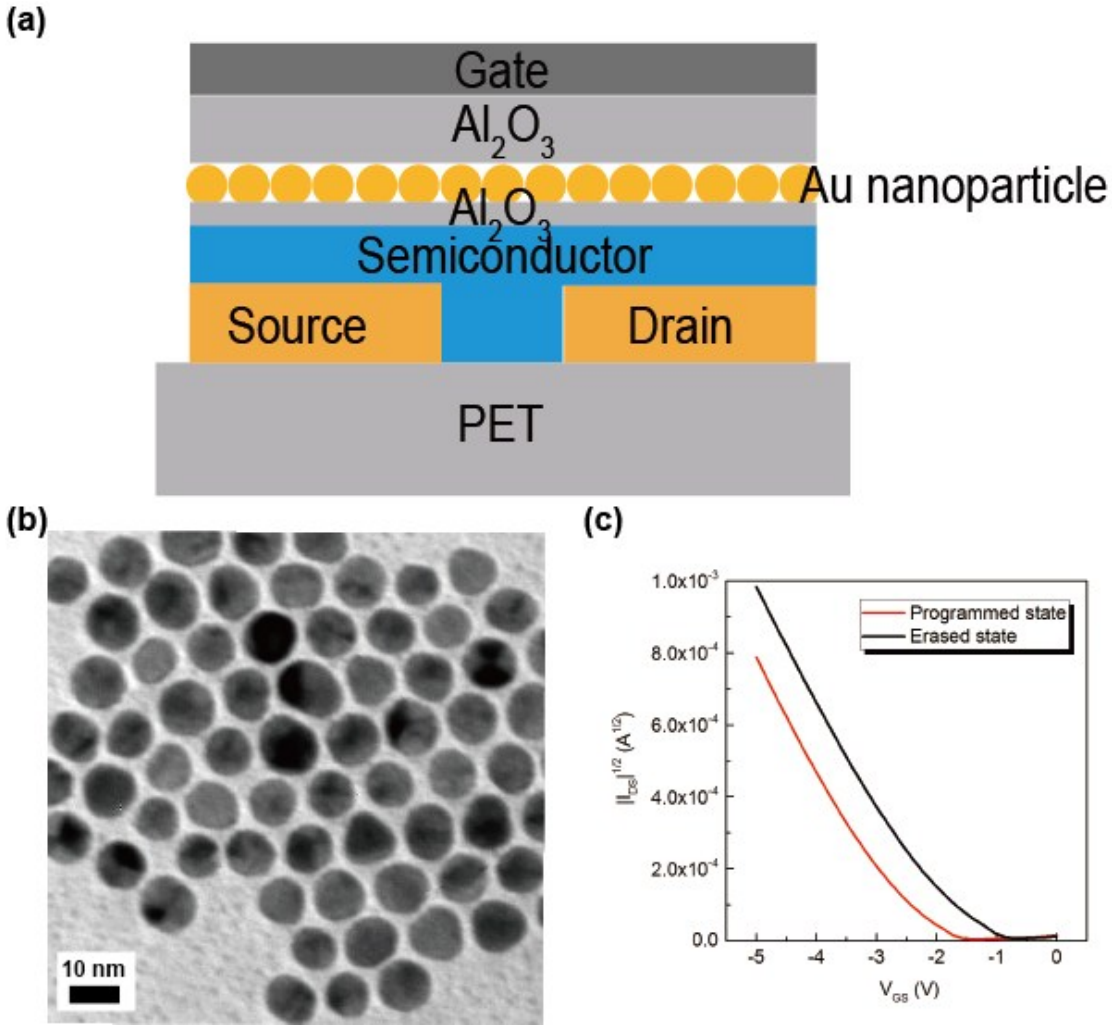

Fig. S4. (a) Schematic illustration of the top gate/bottom contact memory transistor with Au nanoparticles. (b) TEM image of Au nanoparticles. (c) The transfer curves of the programmed and erased states at room temperature. The P/E voltage is -5 V/+5 V for 1 s.

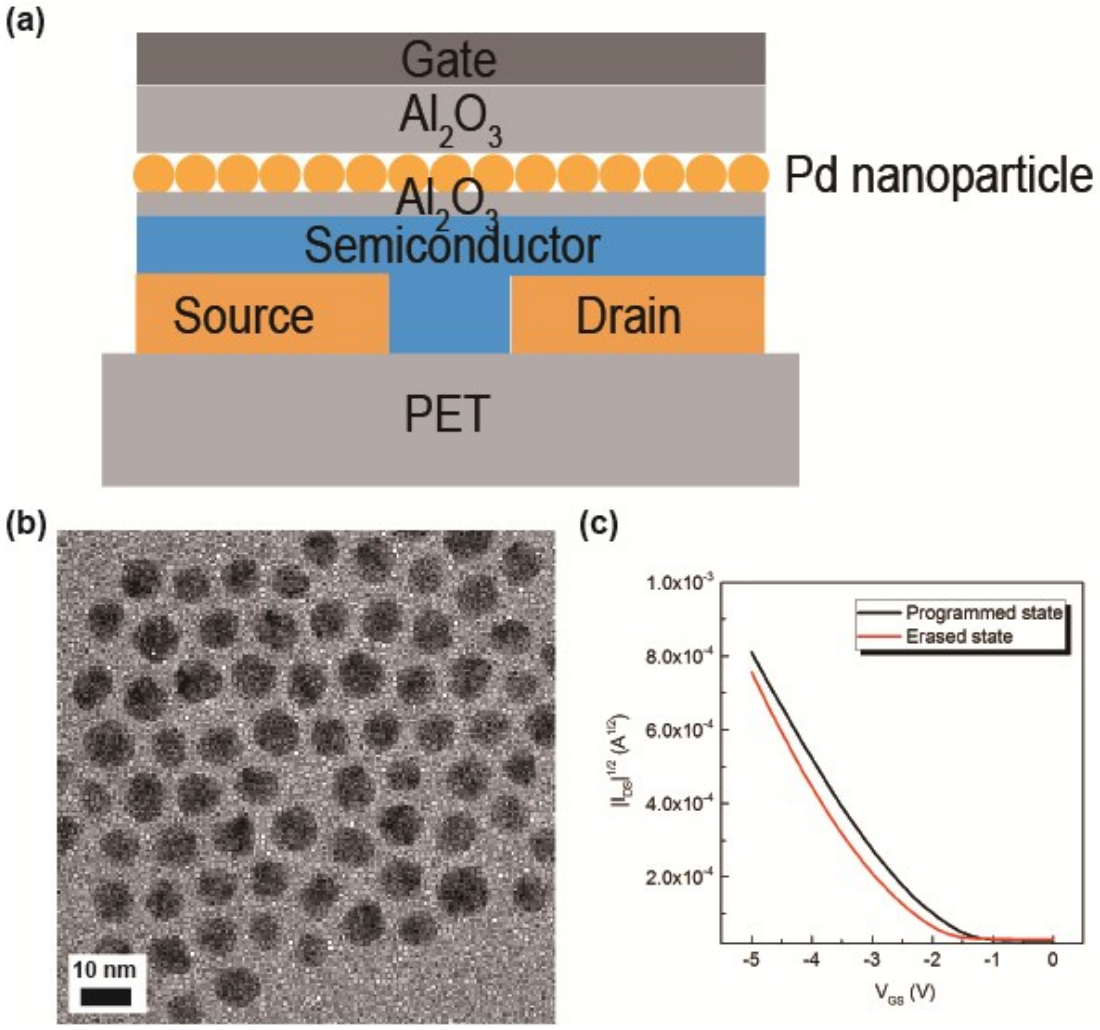

Fig. S5. (a) Schematic illustration of the top gate/bottom contact memory transistor with Pd nanoparticles. (b) TEM image of Pd nanoparticles. (c) The transfer curves of the programmed and erased states at room temperature. The P/E voltage is -5 V/+5 V for 1 s.

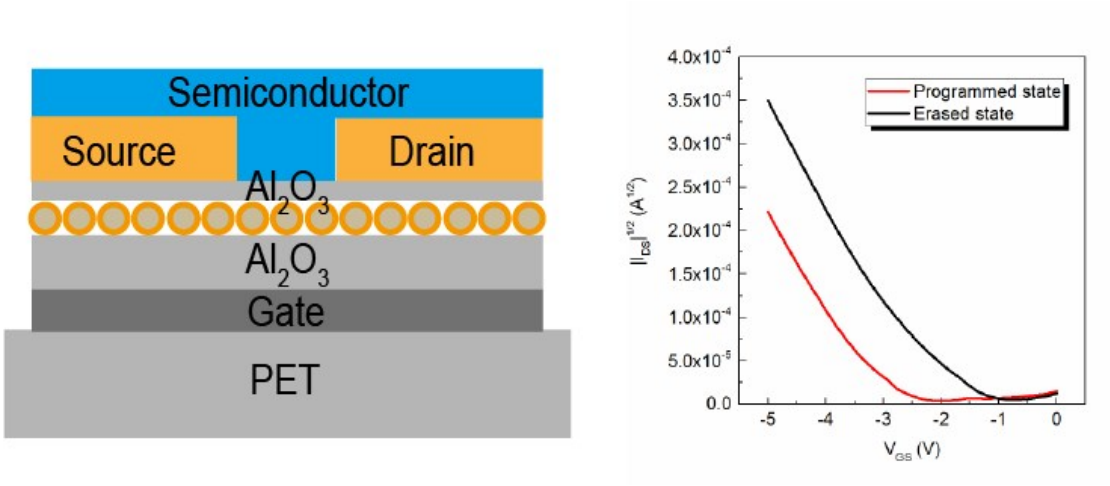

Fig. S6. Schematic illustration of the bottom contact/bottom gate memory transistor and the transfer curves of the programmed and erased states at room temperature.

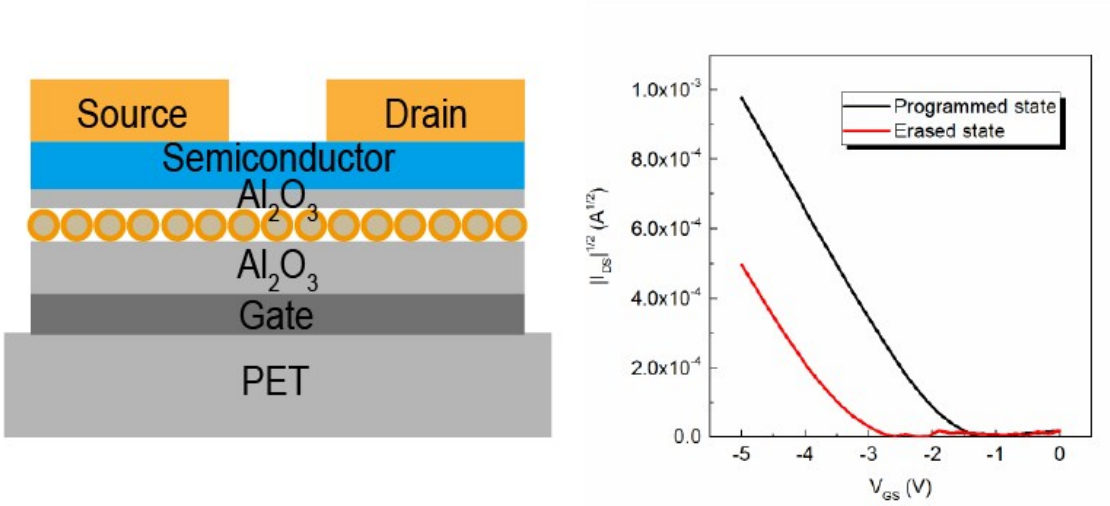

Fig. S7. Schematic illustration of the top contact/bottom gate memory transistor and the transfer curves of the programmed and erased states at room temperature.

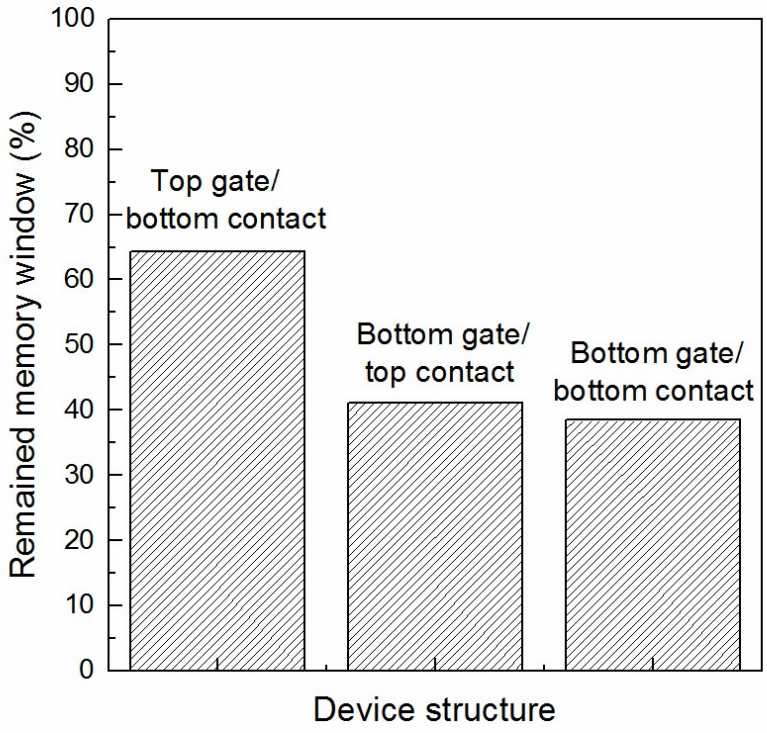

Fig. S8. The data retention comparison between the memory transistors based on various device structures.

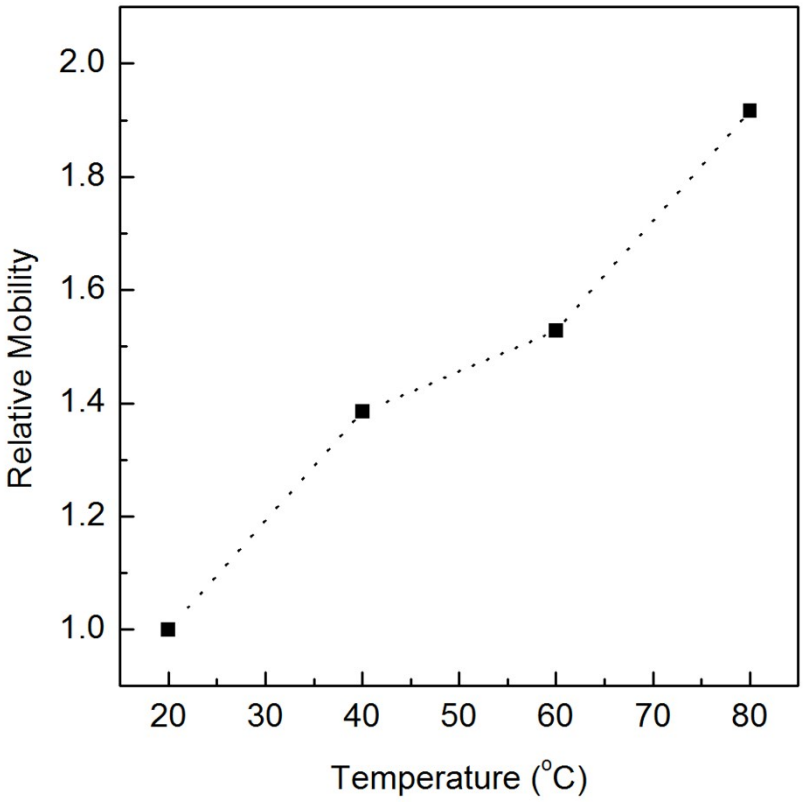

Fig. S9.The relative mobility with respect to different thermal signals.

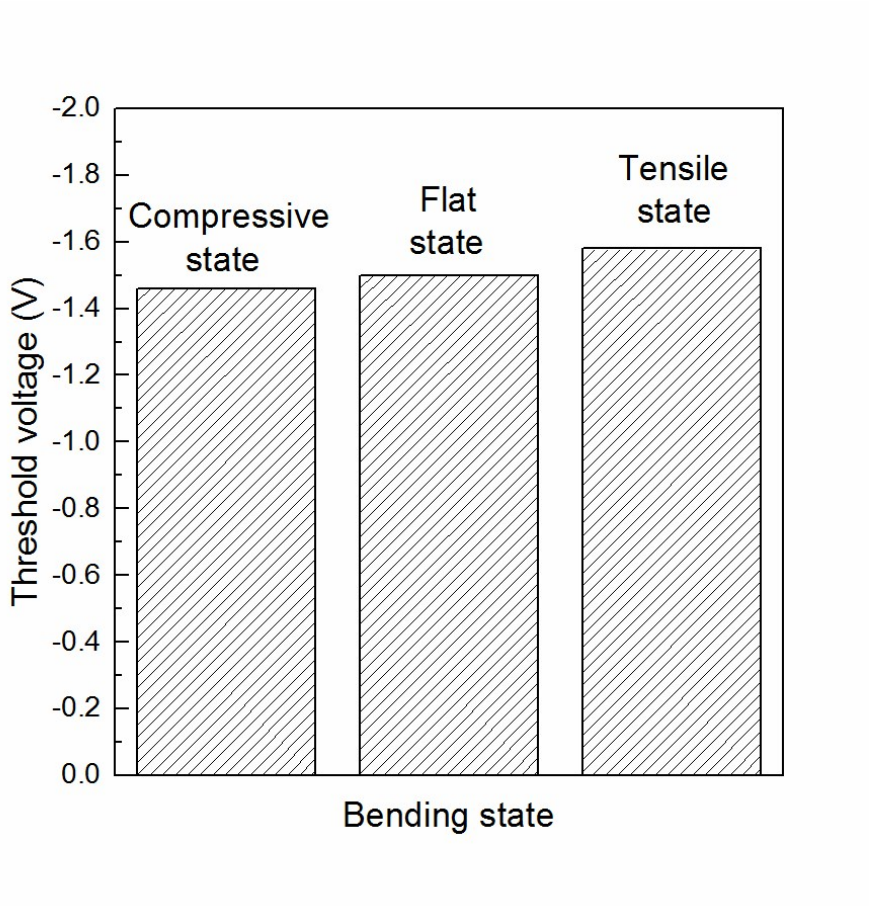

Fig. S10. The programmed threshold voltage of the thermal memory at various bending states. The bending radius is 1 cm.

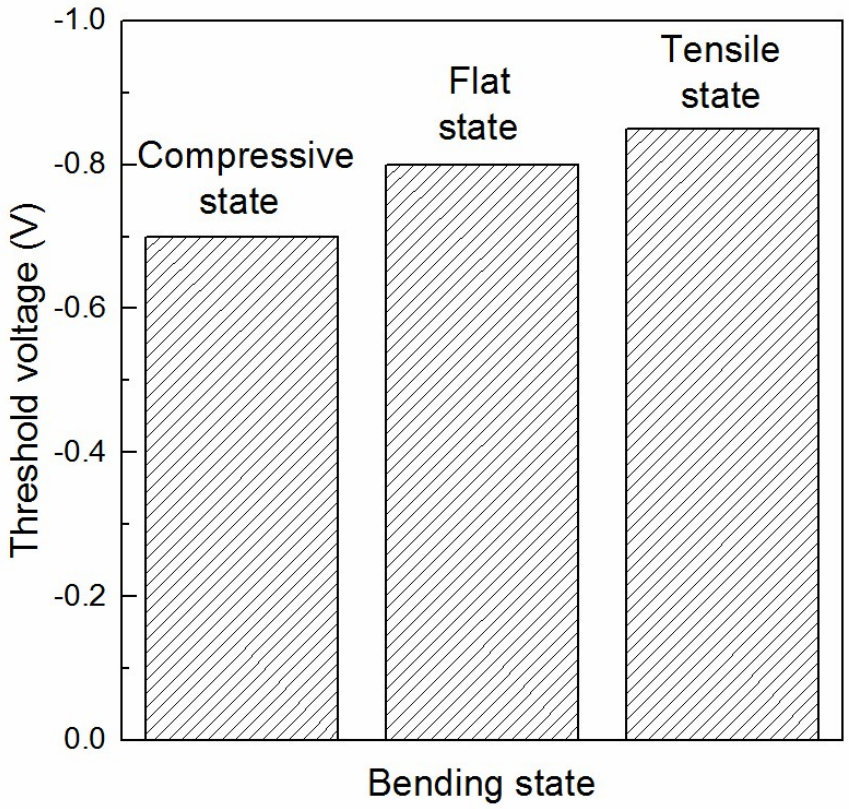

Fig. S11. The erased threshold voltage of the thermal memory at various bending states. The bending radius is 1 cm.