Supporting Information

Polymer transistor arrays with pressure-sensitive elastomers for electronic skin

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Experimental Details

Fabrication of OFET

To fabricate the bottom part of OFET, first the patterned Au (thickness 40 nm) was deposited on SiO_2-coated silicon substrate by thermal evaporation through a shadow mask to form the source and drain electrodes. Then, the semiconducting polymer PCDTPT (1-Material) was spin-coated (1000 rpm, 60 s) on the substrate using the solution concentration of 4mg/mL in chlorobenzene. The polymer film was annealed at 200°C to obtain the optimum performance of OFET. The channel length and width of the OFET is 100 μm and 4000 μm, respectively.

To fabricate the top part of the OFET, the following steps were carried out. The part A and part B of Ecoflex 0030 (from Smooth-On) were mixed in 1:1 ratio and degassed in the vacuum to eliminate the trapped air. The mixture was then coated on a cleaned and UV-ozone-treated ITO-coated PET film by doctor blading. The thickness of the Ecoflex film was controlled by the thickness of the spacer. The Ecoflex film was first cured at room temperature for 1 hour, followed by 80 °C for 2 hours and 100°C for 1 hour. For PDMS-based OFET, PDMS (Sylgard 184, Dow Corning) was mixed with cross-linker in 10:1 ratio (degassing in vacuum is required to remove the air bubble after mixing) and diluted with hexane (10 wt%). The PDMS solution (~ 100 μL) was dropped on a wafer which is pre-treated with octadecyltrichlorosilane. An ITO-coated PET film (Xinyan Technology Ltd) was cleaned, UV-ozone-treated and placed on the PDMS solution. After placing the ITO-coated PET film, the PDMS solution nicely spreads on the wafer and thin layer of PDMS solution was formed between the wafer and the ITO-coated PET film. Then, the entire stack was put in an oven at 80 °C for overnight to cure the PMDS. After curing, the PDMS

film could be easily removed from the wafer due to the octadecyltrichlorosilane treatment but it firmly attached to the ITO-coated PET.

To assemble the OFET, the top part was laminated on the bottom part (elastomer and PCDTPT are facing each other) by hot-pressing them against each other while sandwiching between the two sheets of lamination pouch.

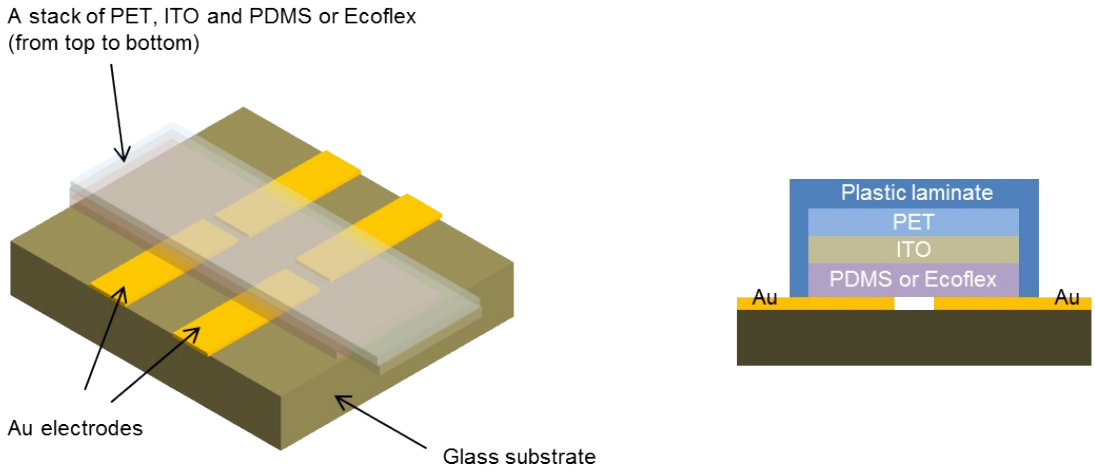
Fabrication of parallel-plate capacitor

The Au electrodes were deposited on a pre-cleaned glass substrate by thermal evaporation through a shadow mask. The elastomers were deposited on the ITO-coated PET film using the same procedures mentioned in the OFET fabrication. The two parts were assembled by lamination process (See Figure S1).

Characterization

Both capacitance and OFET were tested using Keithley semiconductor parametric analyser (Keithley 4200) in ambient conditions. The pressure was applied by manually loading the weight on the device. The pressure is calculated by the relationship; $P = F/A$ where P, F and A are the pressure, force and area of surface on contact. The force is calculated using; F = mass × acceleration due to gravity (9.8 m/s^2, approximately equal to 10 m/s^2).

(a)



(b)

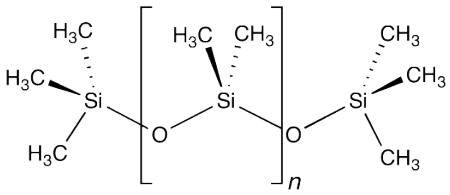


Figure S1. (a) The device structure of the parallel-plate capacitor which is used for the pressure sensitivity test. The area of each capacitor is ~ 10mm^2 which is determined by the area overlap between the Au electrode and ITO electrode. (b) The chemical Structure of PDMS.

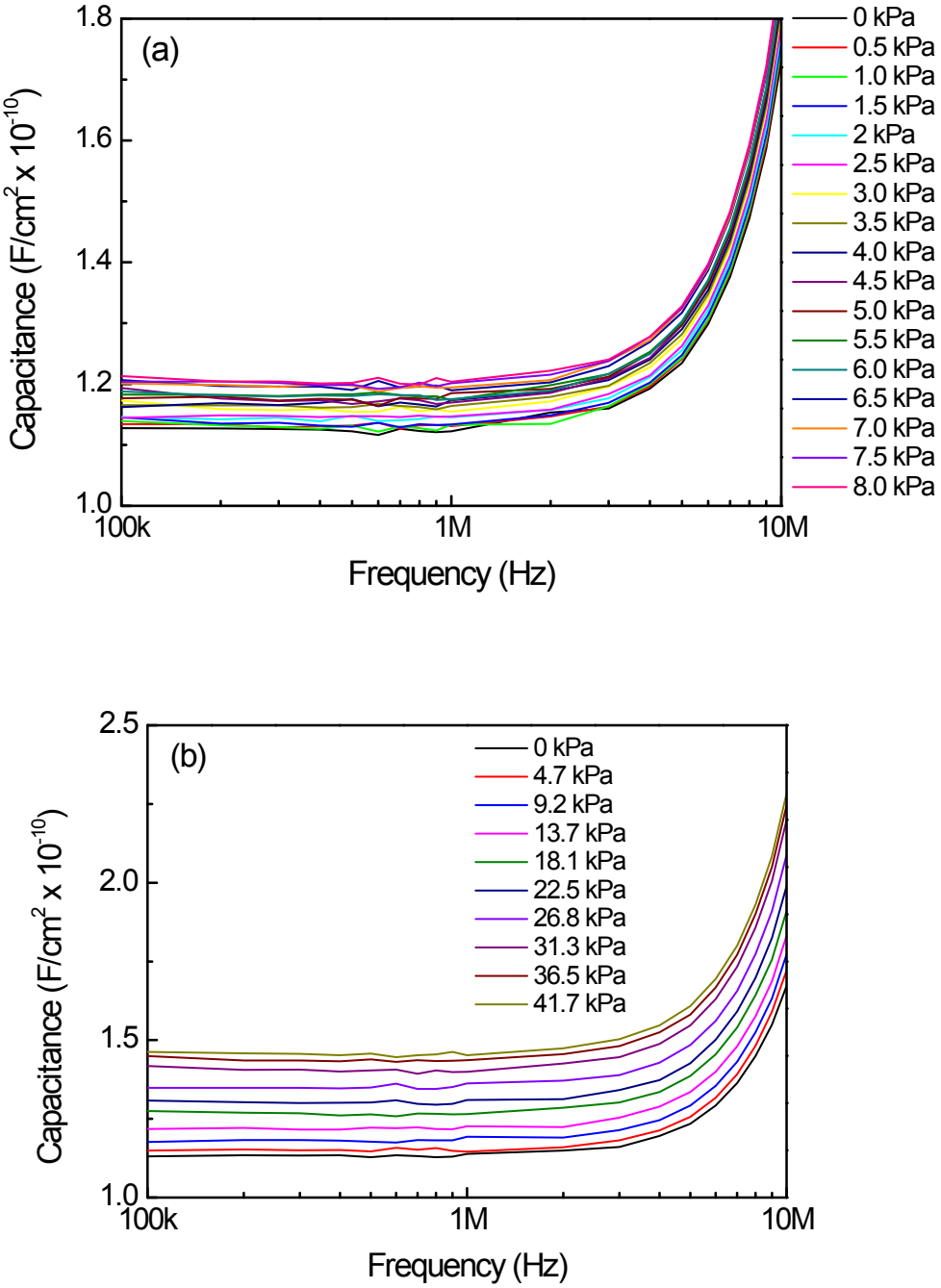


Figure S2. The capacitance of the parallel-plate capacitor with Ecoflex elastomer for various applied pressure (a) from 0 kPa to 8 kPa with increment of 0.5 kPa, and (b) from 0 kPa to 42 kPa with increment of ca. 4.5 kPa.

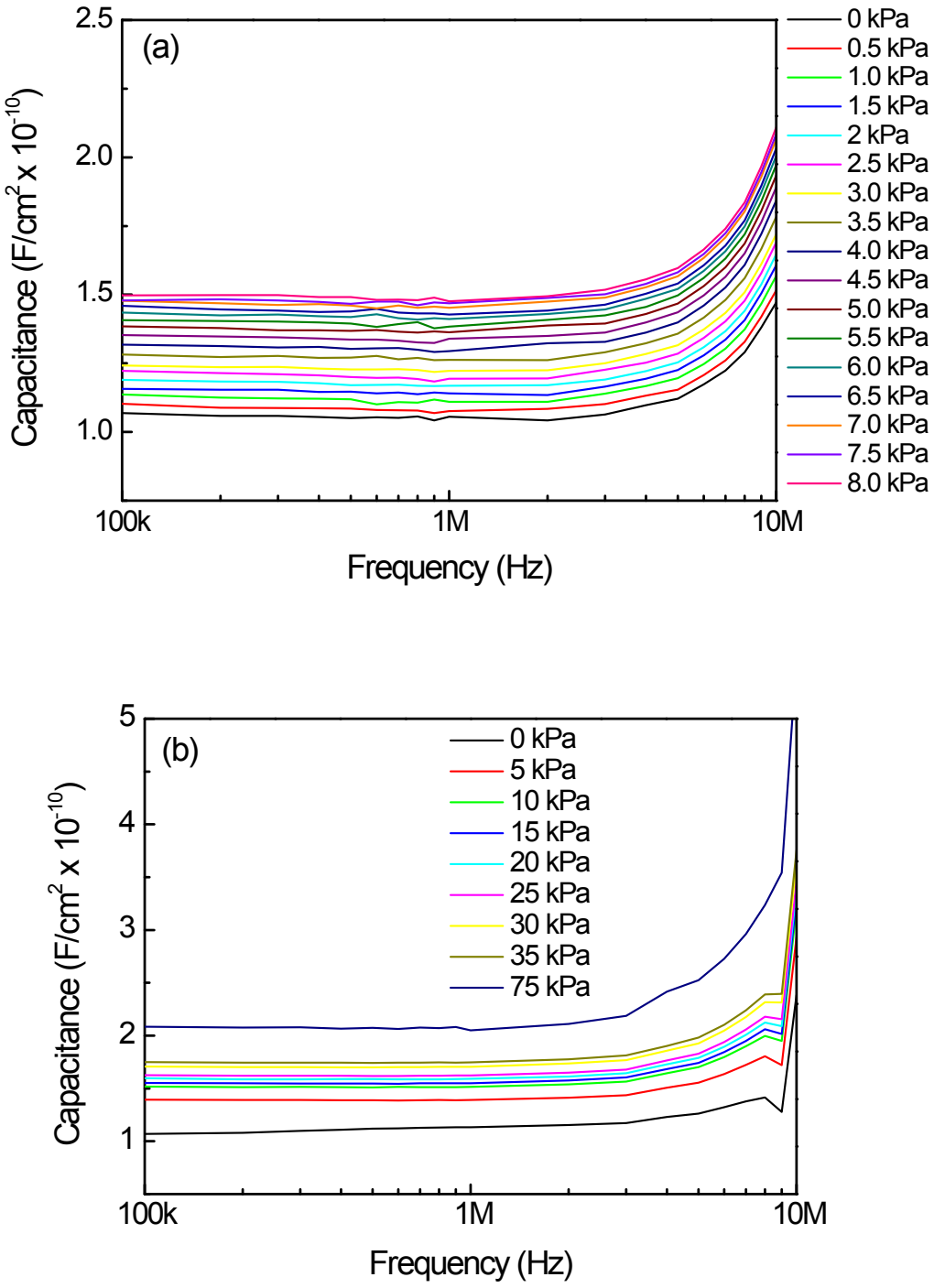


Figure S3. The capacitance of the parallel-plate capacitor with PDMS elastomer for various applied pressure (a) from 0 kPa to 8 kPa with increment of 0.5 kPa, and (b) from 0 kPa to 35 kPa with increment of 5 kPa, and at 75 kPa.

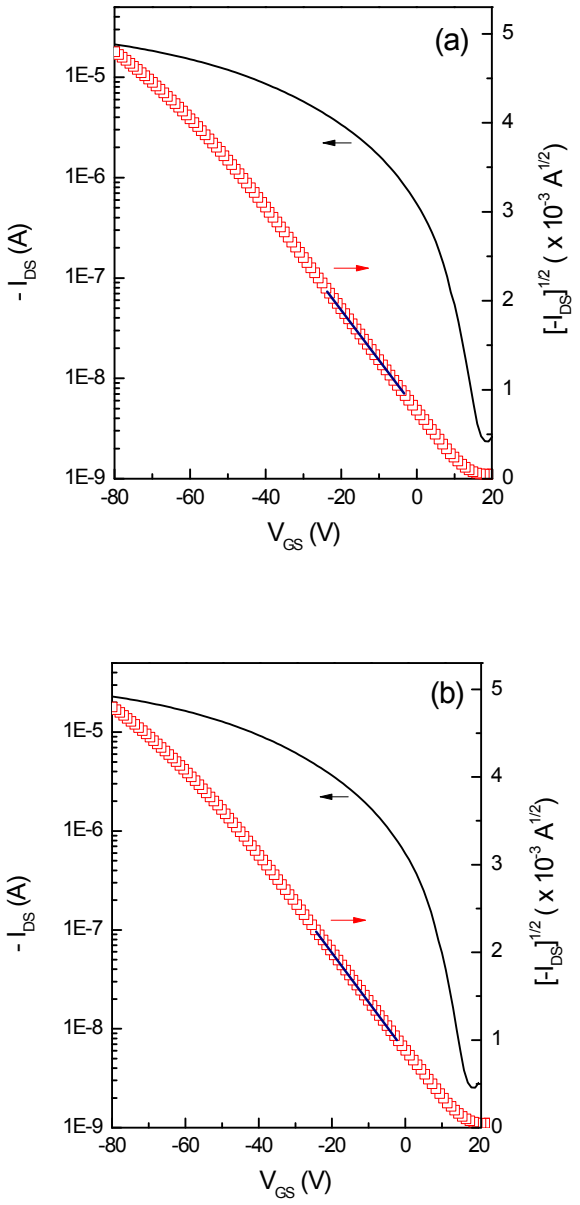


Figure S4. The transfer characteristic of OFET with Ecoflex (a) and PDMS (b) elastomer at zero applied pressure and V_{DS} = -80V. The mobility is extracted from the slope of the square root of I_{DS} Vs V_{GS} in low V_{GS} region (between -10V and -20V).

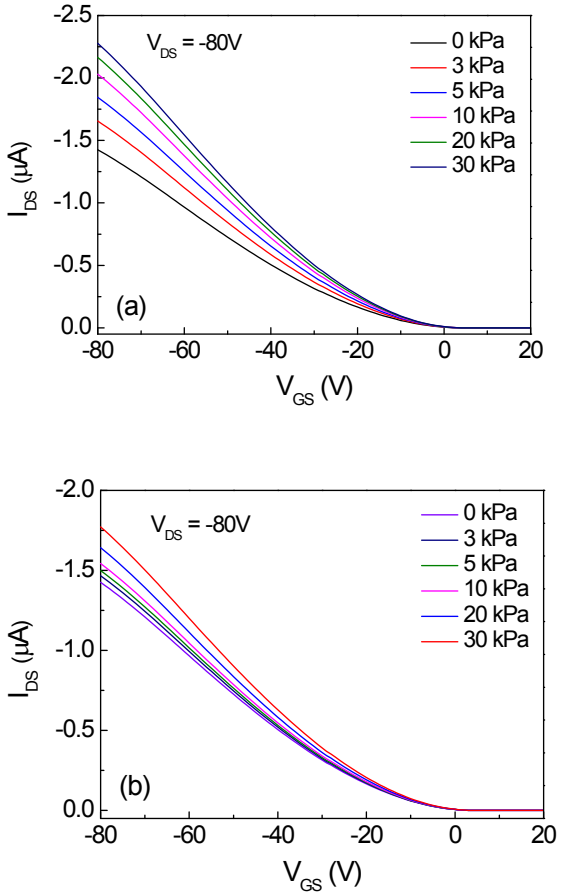


Figure S5. The transfer curve (I_{DS} *vs* V_{GS}) of P3HT-based OFET with PDMS dielectric layer (a) and Ecoflex dielectric layer (b).

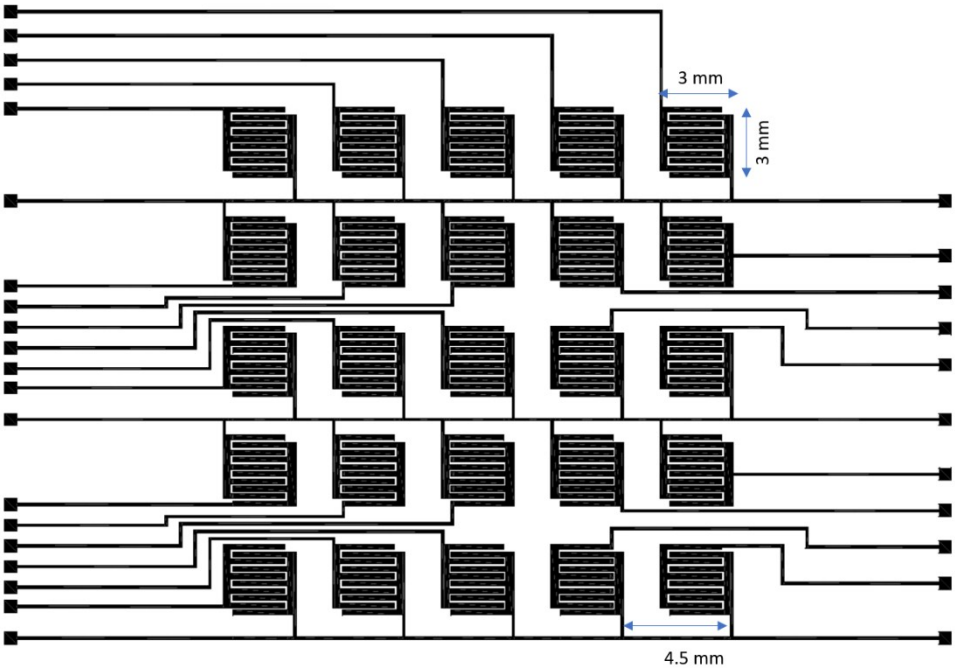


Figure S6. The design of a complete pixel array with detailed dimensions.

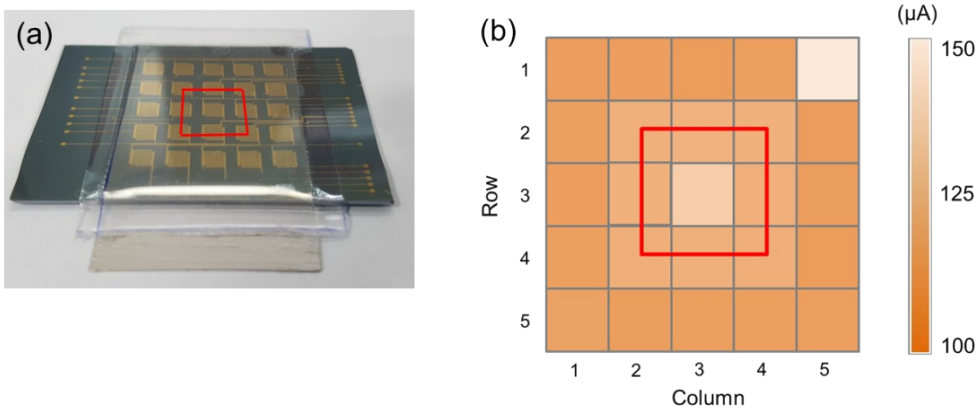


Figure S7. (a) The photograph of the e-skin with a 5 × 5 pixel array. The red lines represent the area where the square block is placed; the edges of the object lay on the pixels. (b) The corresponding pressure image obtained from the drain current measurement.