

Electronic Supplementary Material (ESI)

**Cu-Doped Nickel Oxide Prepared by Low-Temperature Combustion Method as a Hole-Injection Layer
for High-Performance OLEDs**

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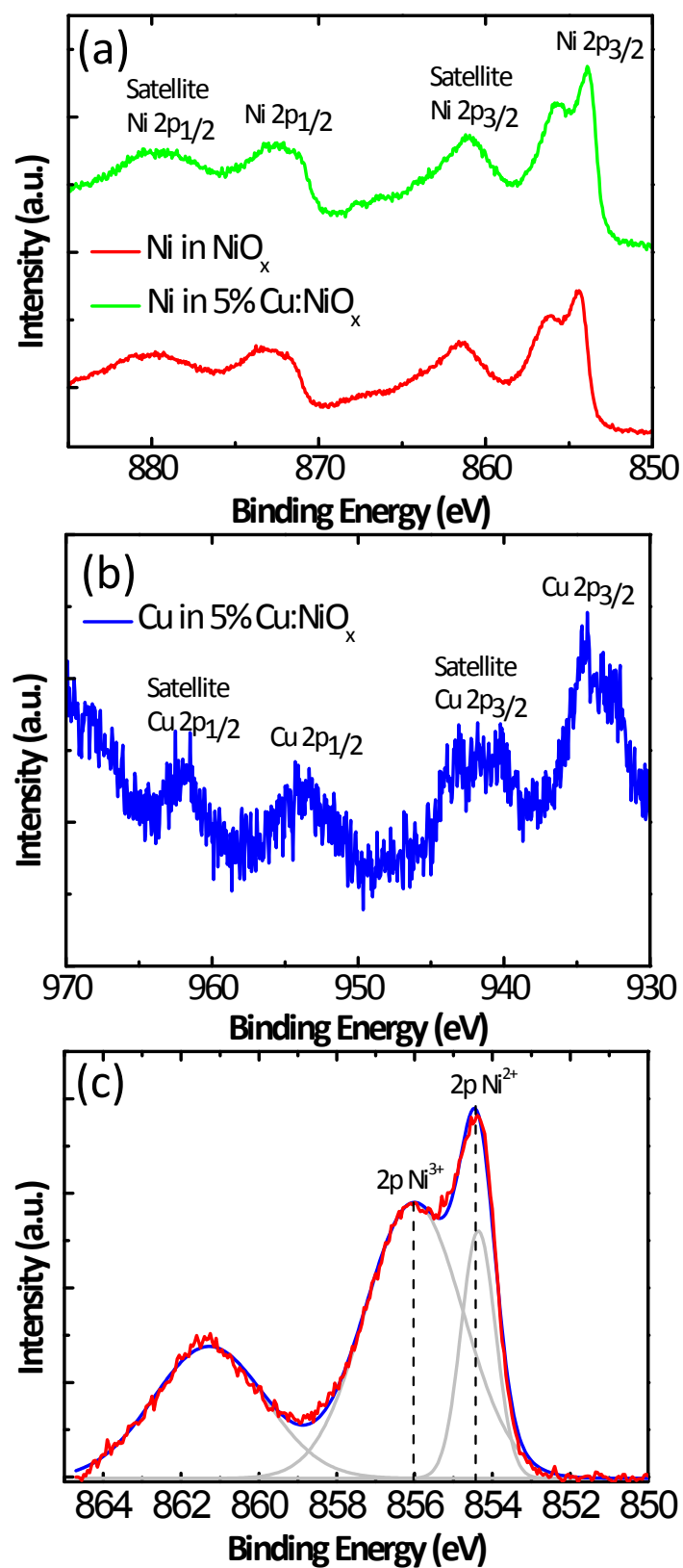


Fig. S1. XPS spectra showing Ni 2p (a) and Cu 2p (b) core levels of NiO_x and (5 mol%) Cu:NiO_x thin films prepared by combustion method. XPS results of Ni 2p 3/2 with curve fitting (c). s-NiO_x and s-Cu:NiO_x films were subjected to 200 °C annealing treatment.

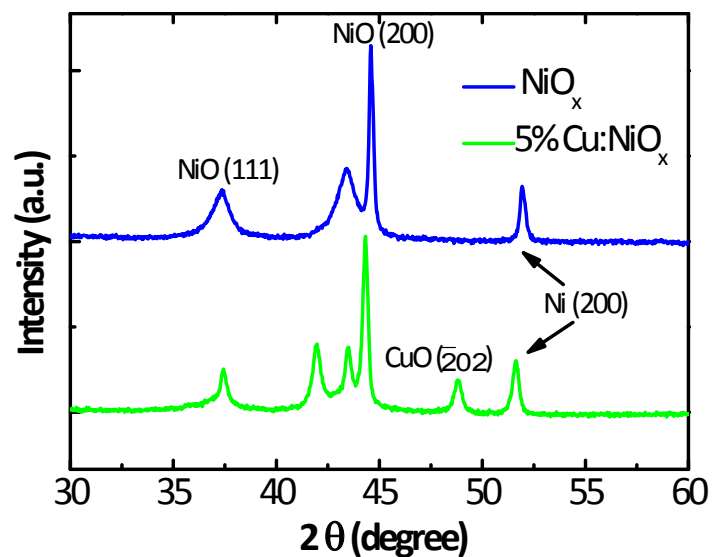


Fig. S2. XRD patterns of s-NiO_x and (5 mol%) s-Cu:NiO_x films (200 °C annealed)

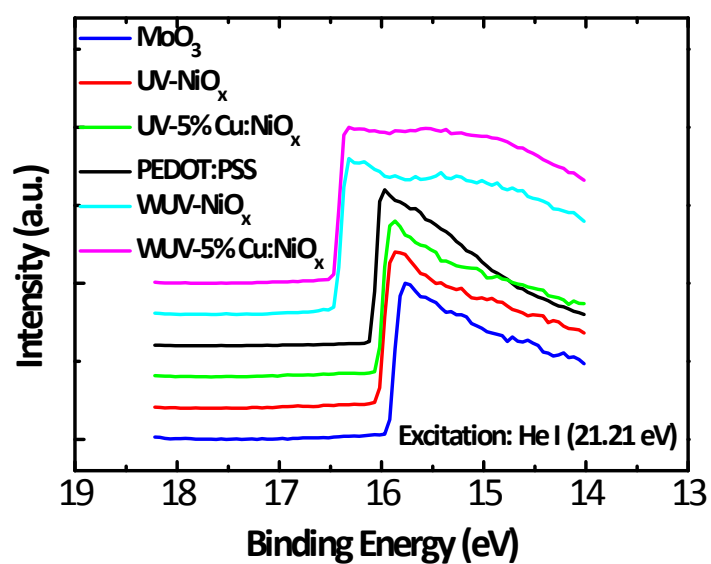


Fig. S3. The secondary cutoffs of the UPS spectra of PEDOT:PSS, MoO₃, s-NiO_x (200 °C annealed) and (5 mol%) s-Cu:NiO_x films (200 °C annealed) with/without UV-ozone treatment.

CA left: 4.6°
CA right: 4.6°

(a)

CA left: 17.2°
CA right: 17.2°

(b)



Fig. S4. Photographs showing the water contact angle for the UV-ozone treated (a) and untreated (b) s-NiO_x films.

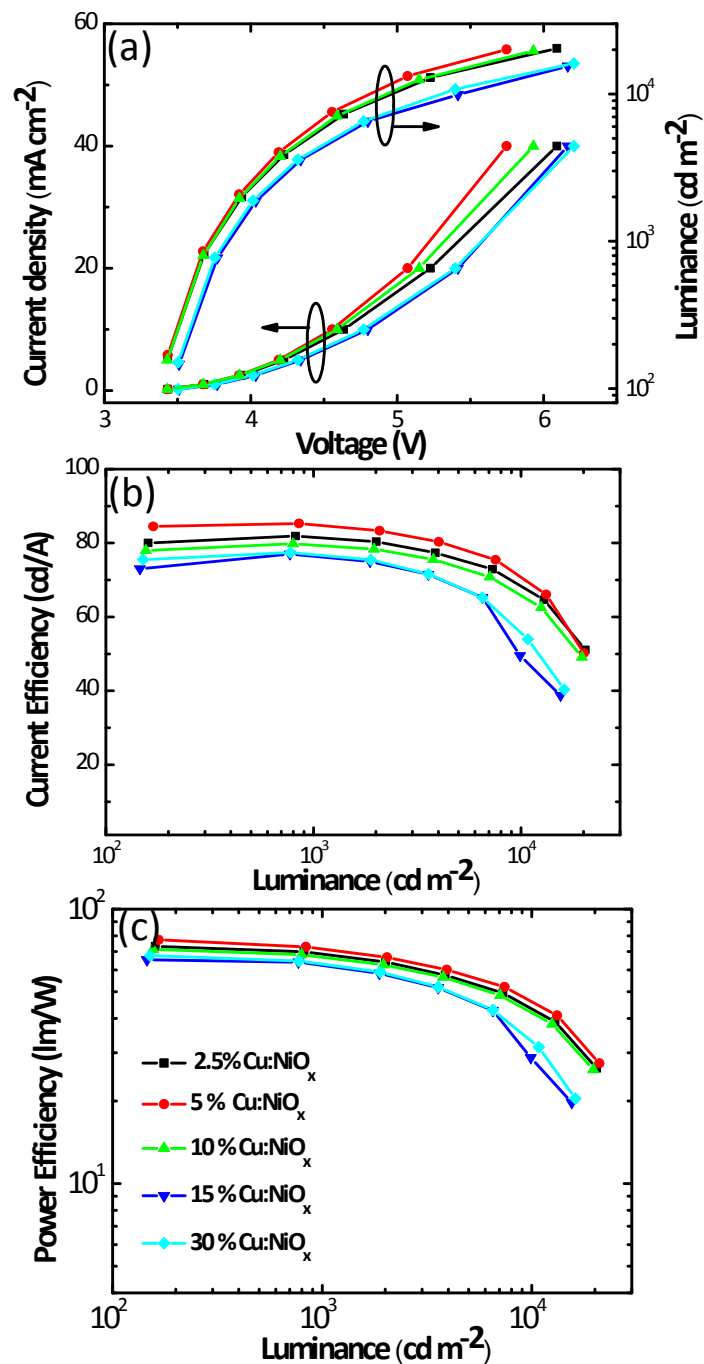


Fig. S5. (a) J-V-L characteristics and (b,c) Current efficiency-power efficiency-luminance characteristics of devices with different Cu doping ratios of s-NiO_x films.

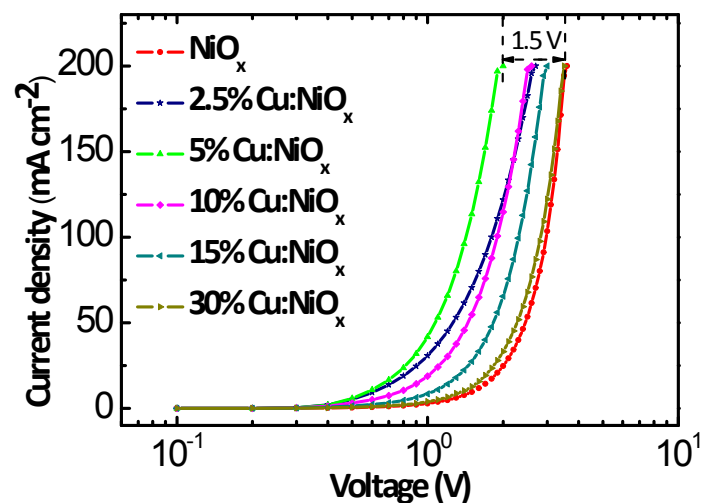


Fig. S6. J–V characteristics of doped NiO_x based hole-only devices with the structure: ITO/HIL (30 nm) /TAPC (40 nm)/TCTA (20 nm)/ MoO_3 (20 nm)/Ag (100 nm). A non-doped device was also fabricated for reference.

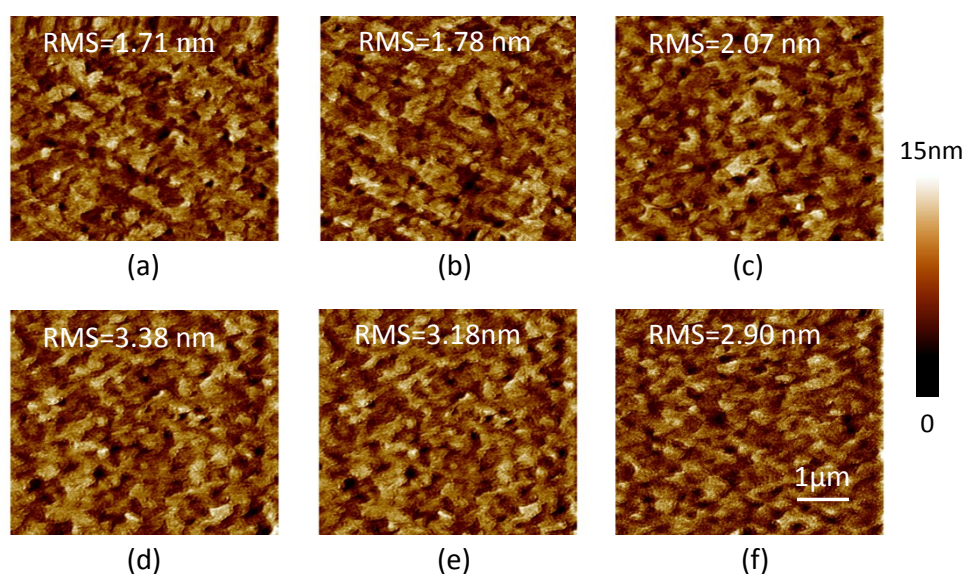


Fig. S7. AFM images of different ratios of Cu (0 – 30 mol%) doped s- NiO_x films. The Cu doping ratios at 0% (a), 2.5% (b), 5% (c) 10% (d), 15% (e) and 30% (f). The measured area is $5 \times 5 \mu\text{m}$.

Table S1. Energy levels of different materials used in this work.

	NiO_x	5% Cu: NiO_x	PEDOT:PSS	MoO_3	TAPC
WF.	5.19eV	5.18eV	5.12eV	5.32eV	
Ref.			5.1/5.2eV	5.3/5.4eV	5.5eV ^a

^a HOMO of TPAC.

Table S2. A summary of OLED performance based on different HTLs.

Device ^a ,	V ^b [V]	CE ^c [cd A ⁻¹]	PE ^c [lm W ⁻¹]
NiO _x	4.08,4.68	72.5,71.6,63.7	61.0,42.1,27.3
5% Cu:NiO _x	4.04,4.62	74.8,74.5,67.1,	62.9,45.4,29.5
TAPC	4.19, 4.81	67.5,65.7,61.8	56.9,45.5,36.3

^a Devices using different HTLs. ^b Driving voltage at 500 cd m⁻² and 2000 cd m⁻².

^c Current and power efficiencies in the order of maximum, at 1000 cd m⁻² and at 5000 cd m⁻².