Supporting Information

Solution-processed ternary p-type CuCrO$_2$ semiconductor thin films and their application in transistors

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The O 1s binding energies of the $CuCr_xO_y$ thin films annealed at various temperatures are shown in Figure S1(a). The O 1s peaks were divided into two peaks centered at 529.5 eV and 531.8 eV, which can be assigned to the lattice oxygen and the oxygen defects (insertion of O^{2-} ions herein) in $CuCr_xO_y$ thin films,[1] respectively. From the thin films annealed at 500 °C to 600 °C, the lattice oxygen component increases with increasing annealing temperature because the oxygen-related defects are eliminated and the M-O bonds are enhanced with the increase of the annealing temperature.[2] However, the decrease of the lattice oxygen component from 600 °C to 700 °C may be due to the transformation from mixed $CuCr_2O_4$ and CuO phase to pure $CuCrO_2$ phase. This process may be accompanied by the breakdown of the M-O bonds and the release of the oxygen, leading to the decrease of M-O component. Reasonably, the M-O component experienced an increase from 700 °C to 900 °C, resulting from the improvement of $CuCrO_2$ phase crystallinity.[3]

The Cr $2p_{1/2}$ and Cr $2p_{3/2}$ peaks are located at 586.0 and 576.0 eV, respectively. No apparent change of peak position is observed within the whole processing temperatures (Figure S1(b)), suggesting that Cr^{3+} is maintained during the entire reduction process.

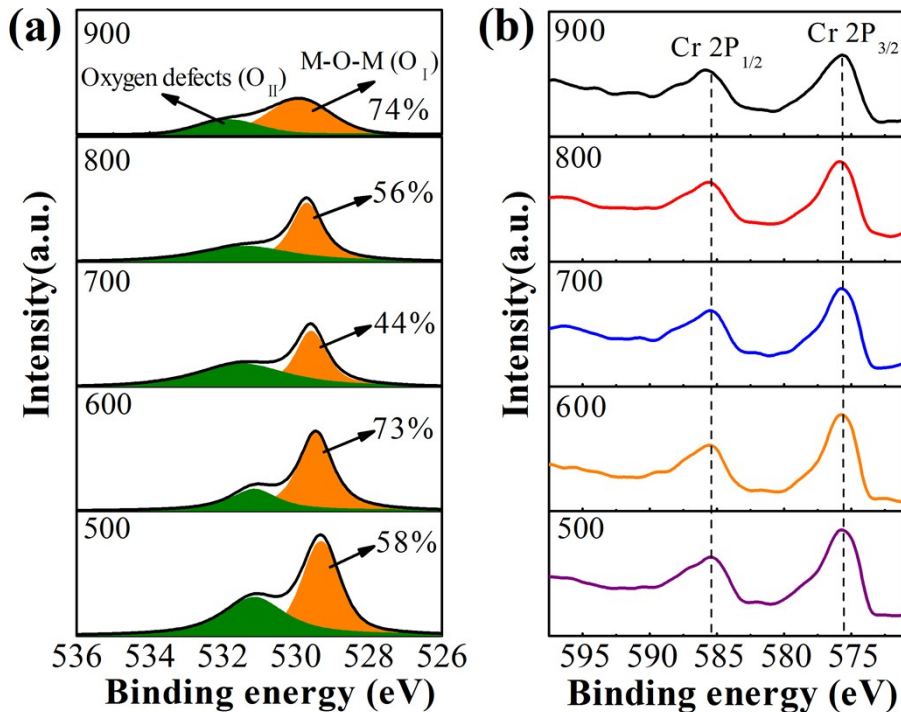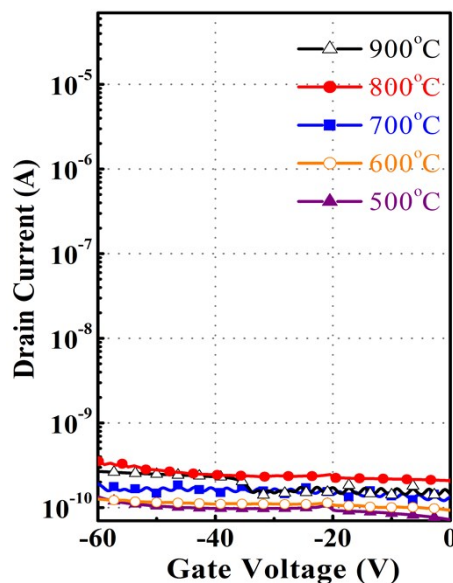Figure S1. XPS (a) O 1s peak and (b) Cr 2p of $CuCr_xO_y$ thin films annealed at various temperatures.

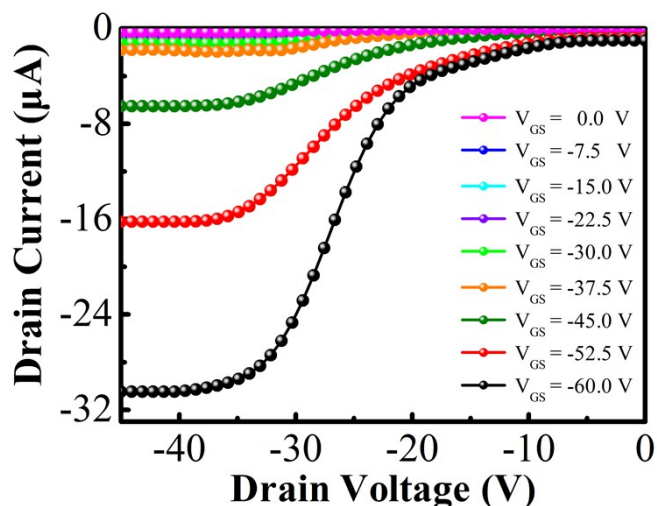Figure S2. Gate leakage current of the $CuCr_xO_y$ TFTs annealed at various temperatures.

Figure S3. The output curves of $CuCrO_2$ TFT annealed at 800 °C.

The output curves exhibit the slight current crowding in the low V_{DS} region and current saturation in the high V_{DS} region. The current crowding phenomenon indicates the Schottky contact between the electrodes and $CuCrO_2$ channel layer, although the Ni metal used in this study possesses high work function (>5 eV). In the previous reports on p-type TFTs, such a Schottky contact behaviors were frequently observed even using other metal electrodes (e.g., Au and Ti/Au bilayer).[4-6] The further optimization of electrode materials is required to achieve ideal Ohmic contact and better device performance.
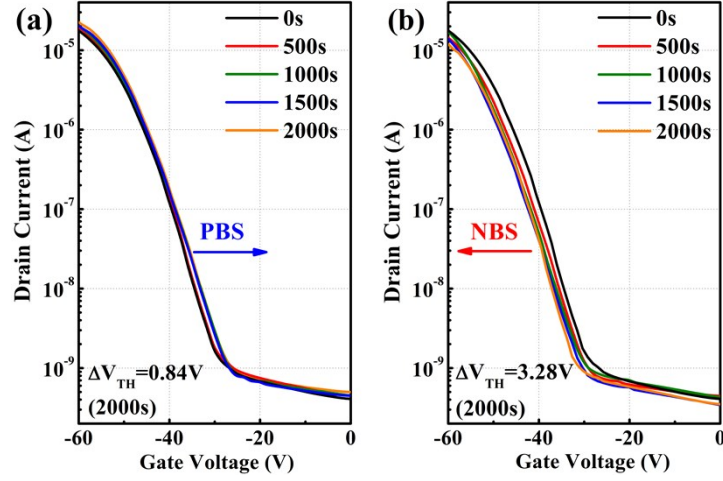
Figure S4. Transfer curves of the CuCrO$_2$ TFTs annealed at 800°C (a) under PBS tests and (b) NBS tests for 2000 s with a time interval of 500 s.

To clarify the gate-bias-stability of the device, both positive bias stress (PBS) and negative bias stress (NBS) measurements were carried out on the optimized CuCrO$_2$ TFT by applying a V_{GS} of ± 60 V. A maximum V_{TH} shift of 0.84 and 3.28 V were recorded after PBS and NBS tests for 2000 s. The main mechanism for the V_{TH} shift is due to the charge trapping effect at the interface.[7] It is noted that the I_{on} of the device degrades gradually with increasing the bias stress time under NBS, while I_{on} remains unchanged under PBS tests. For the p-type oxide TFTs, the amount of electrons in channel layers is negligible compared with holes. Under NBS test, the interface states are gradually filled with the increase of the stress time. The trapped holes at CuCrO$_2$ interface will possibly induce either phonon scattering or Coulomb scattering, leading to the decrease of I_{on}.[8]

Table S1. Chemical compositions of CuCr$_x$O$_y$ thin films annealed at various temperatures.

Temperature (°C)	Cu (at%)	Cr (at%)	O (at%)	C (at%)
400 (air)	20.1	22.2	54.4	3.3
500 (N$_2$)	20.4	22.1	54.3	3.2
600 (N$_2$)	21.3	23.1	52.3	3.3
700 (N$_2$)	21.5	23.0	52.4	3.1
800 (N$_2$)	22.8	22.9	51.0	3.3
900 (N$_2$)	22.5	22.8	51.4	3.3

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