Supporting Information

Hot slot die coating for additive-free fabrication of high performance roll-to-roll processed polymer solar cells

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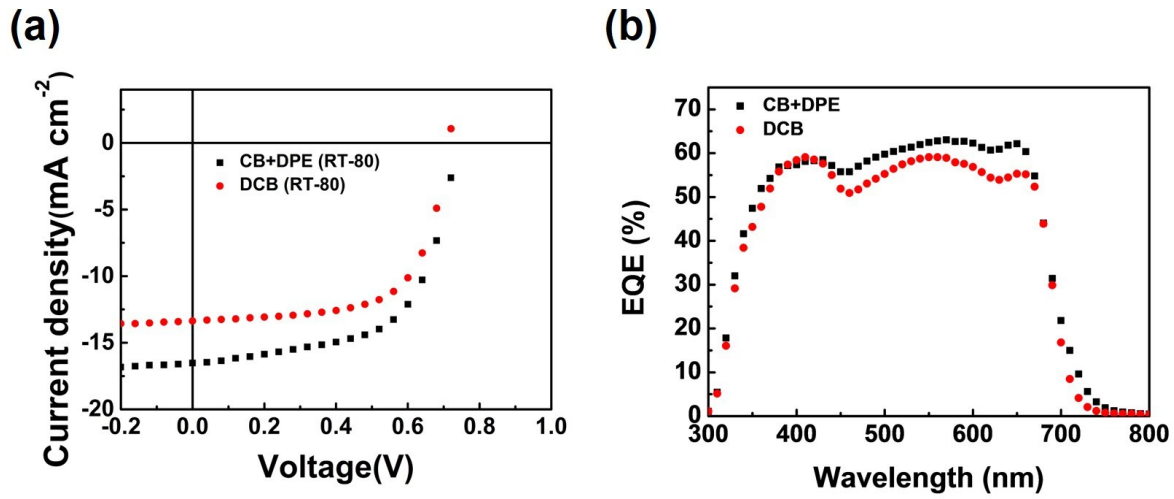

Figure S1. *J-V* characteristics of PPDT2FBT:$PC_{71}BM$-based inverted PSCs with different solvents at a head temperature of 25 ℃ and substrate temperature of 80 ℃ (H25-S80).

Table S1. Detailed photovoltaic parameters at variable processing temperatures.

Solvent	**Temperature of substrates**	J_{SC} **(mA cm^{-2})**	V_{OC} **(V)**	**FF**	**PCE (%)**
CB+DPE	25	12.8	0.69	0.34	2.99
	40	16.4	0.70	0.47	6.12
	60	16.8	0.73	0.52	6.33
	80	16.5	0.74	0.61	7.43
	100	15.8	0.73	0.58	6.13
DCB	25	9.83	0.66	0.54	3.55
	40	11.7	0.71	0.54	4.49
	60	12.2	0.72	0.65	5.65
	80	12.6	0.71	0.65	5.89
	100	7.29	0.73	0.51	2.72

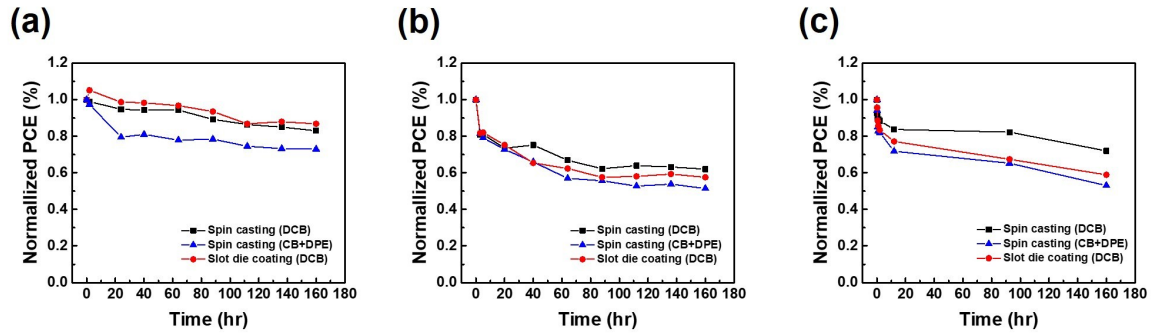

Figure S2. (a) long-term device stabilities in air, (b) thermal stabilities at 120 °C in N_2 filled glove box and (c) photo stabilities under AM 1.5G illumination in air. The photoactive layer of PSCs were spin-coated with and without additives, and also slot die coated for comparisons of devices durability. The devices used for stability testing were encapsulated in glass.

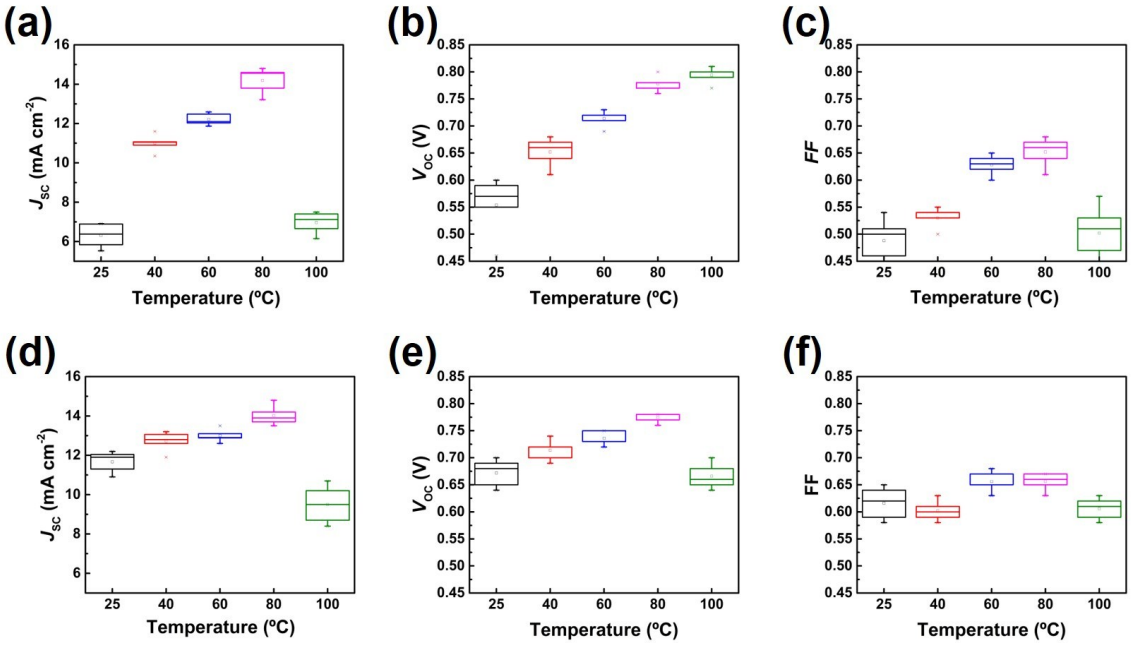

Figure S3. (a-c) J_{SC}, V_{OC} and FF, respectively of devices processed at different substrate temperatures at a fixed slot head temperature of 80 °C. (d-f) J_{SC}, V_{OC} and FF, respectively, of devices processed at different slot head temperatures at a fixed substrate temperature of 80 °C. Each data point and the associated error bars represent the mean value and standard deviation, respectively.

Table S2. Summary of optimal photovoltaic parameters of PSCs processed using various processing temperatures.

Slot head Temperature (°C)	Temperature of substrates (°C)	J_{SC} (mA cm^{-2})	V_{OC} (V)	FF	Best PCE (%)
25	25	7.29	0.62	0.52	2.35
	40	11.1	0.66	0.56	4.06
	60	11.8	0.68	0.60	4.79
	80	12.2	0.70	0.62	5.29
	100	4.77	0.70	0.61	2.41
40	25	7.53	0.61	0.57	2.62
	40	11.2	0.67	0.61	4.57
	60	12.8	0.71	0.60	5.42
	80	13.2	0.74	0.63	6.40
	100	4.20	0.71	0.62	1.84
60	25	6.58	0.62	0.53	2.18
	40	11.4	0.69	0.60	4.72
	60	11.7	0.72	0.65	5.52
	80	13.5	0.75	0.68	6.89
	100	4.98	0.68	0.53	1.76
80	25	6.91	0.70	0.58	2.80
	40	11.6	0.68	0.54	4.26
	60	12.6	0.74	0.65	6.06
	80	14.80	0.78	0.66	7.61
	100	7.50	0.81	0.57	3.16
100	25	9.37	0.69	0.55	3.55
	40	10.9	0.70	0.58	4.38
	60	12.1	0.72	0.61	5.32
	80	10.7	0.70	0.63	4.75
	100	4.95	0.73	0.58	2.10

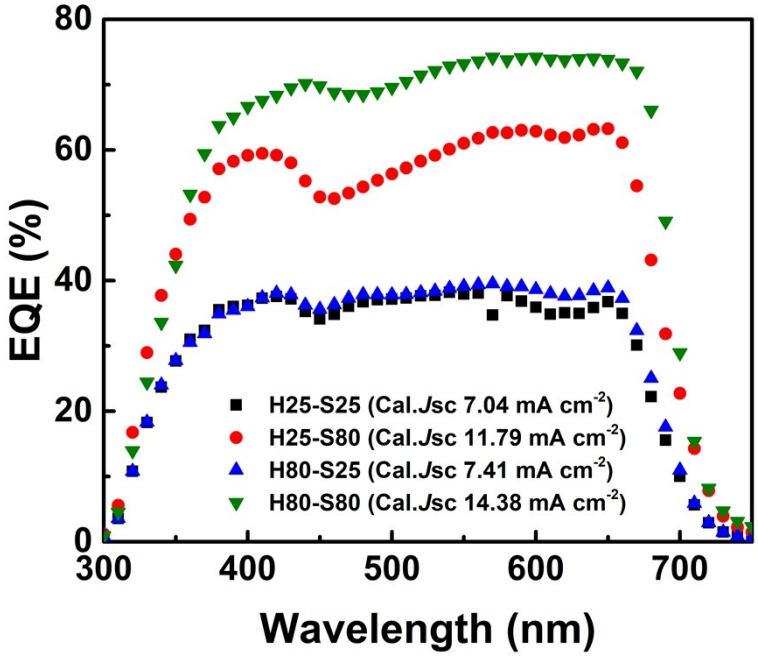

Figure S4. EQE spectra with varying thermal treatment conditions.

Table S3. PSCs performance with various active layer thickness in the H80-S80 process.

Processing condition	Average thickness of films (nm)	J_{SC} (mA cm^{-2})	V_{OC} (V)	FF	PCE (%)
H80-S80	120	13.56	0.78	0.67	7.11
	250	14.92	0.78	0.64	7.42
	500	13.44	0.76	0.63	6.47
	1100	12.31	0.75	0.49	4.54

*Using a 14 mg/ml PPDT2FBT:$PC_{71}BM$ concentration solution, the coating speeds at 3, 11 and 40 mm/s yielded the film thickness of 120, 250 and 500 nm, respectively. The slot die coating at 40 mm /s with 20 mg/ml blend solution yielded ~1100 nm thick films.

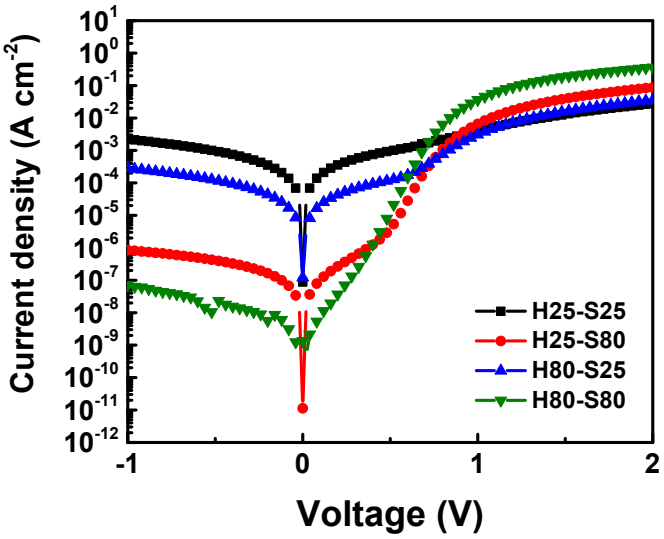

Figure S5. Dark *J-V* characteristics of devices processed at various temperature combination conditions.

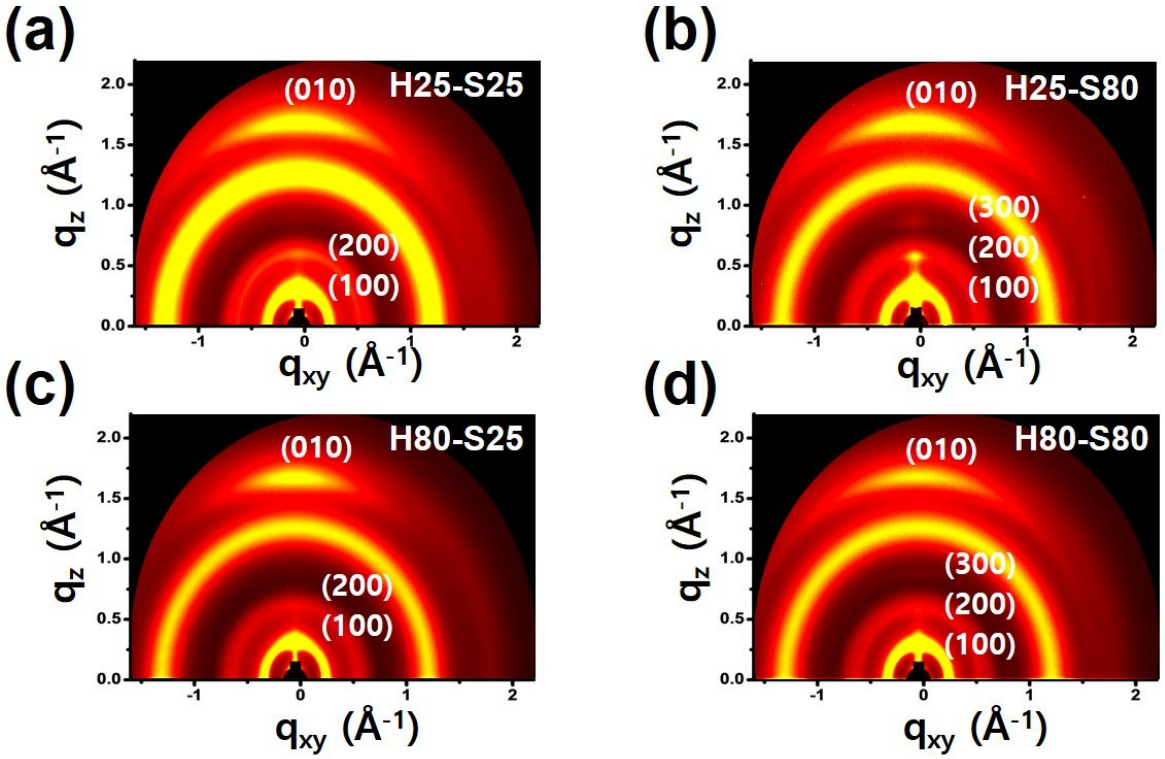

Figure S6. Two-dimensional GIWAXS data for films processed at (a) H25-S25, (b) H25-S80, (c) H80-S25 and (d) H80-S80 conditions, respectively.

Table S4. Crytallographic parameters from GIWAXS data.

Condition	Crystallographic parameters					
	Axis	**π-π stack [Å^{-1}]**	**d-spacing [Å]**	**Coherence length [Å]**	**Lamella stack [Å^{-1}]**	**d-spacing [Å]**
H25-S25	q_{xy}	-	-	-	0.30	20.94
	q_z	1.70	3.70	38.1	0.32	19.63
H25-S80	q_{xy}	-	-	-	0.29	21.67
	q_z	1.70	3.70	41.7	0.30	20.94
H80-S25	q_{xy}	1.90	3.31	45.9	0.31	20.27
	q_z	1.70	3.70	38.6	0.30	20.94
H80-S80	q_{xy}	-	-		0.31	20.27
	q_z	1.70	3.70	44	0.31	20.27

Table S5. PSC performances for comparison of fast cooling and slow cooling after slot die coating.

Slot die coating condition	Cooling condition	Drying time (seconds)	J_{SC} (mA cm^{-2})	V_{OC} (V)	FF	PCE (%)
H80-S60	Slow[a)]	30	9.28	0.75	0.69	4.80
	Fast[b)]	240	7.31	0.72	0.61	3.20
H80-S80	Slow[a)]	5	11.73	0.82	0.69	6.63
	Fast[b)]	23	12.36	0.80	0.62	6.13

a) The substrates after slot die coating were maintained at processing temperature until complete drying.
b) The substrates were cooled to 20 °C right after coating.

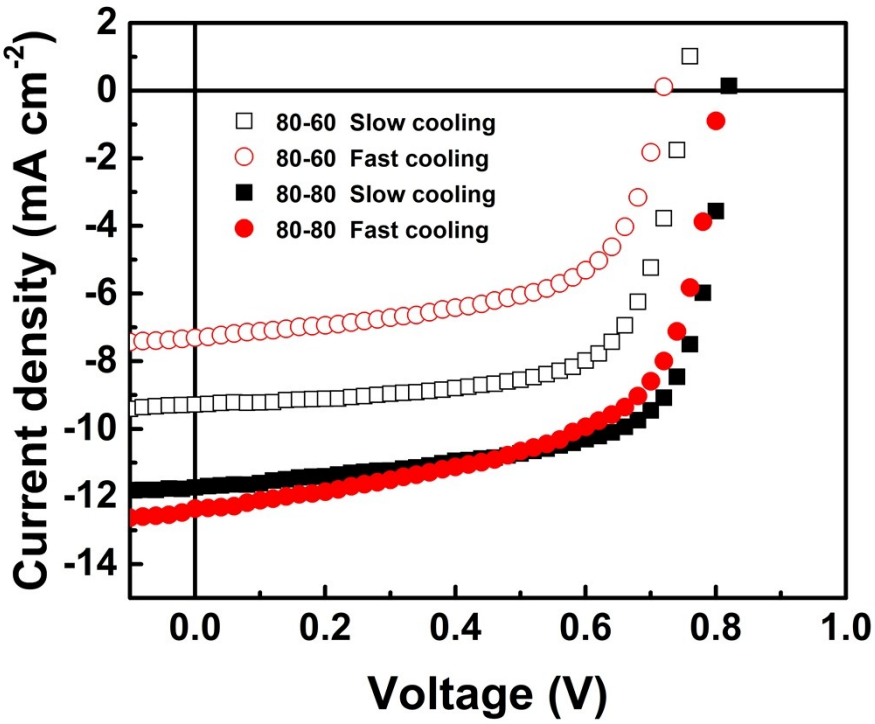

Figure S7. *J-V* curve of fast and slowly dried PSCs at H80-S60 and H80-S80.

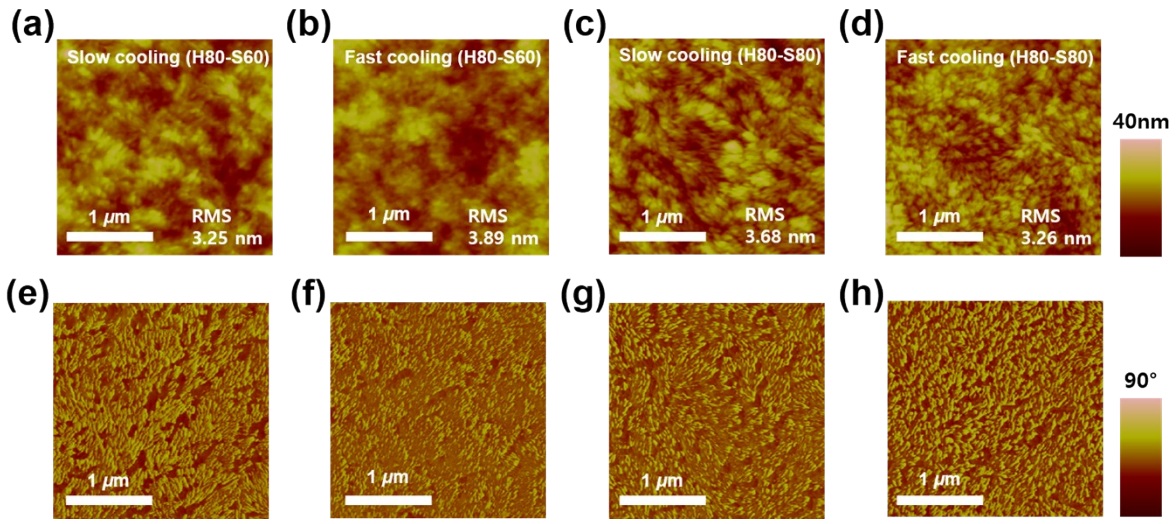

Figure S8. AFM topography (a-d) and corresponding phase images (e-h) for comparison of film morphologies dried by fast and slow cooling after slot die coating at H80-S60 and H80-S80.

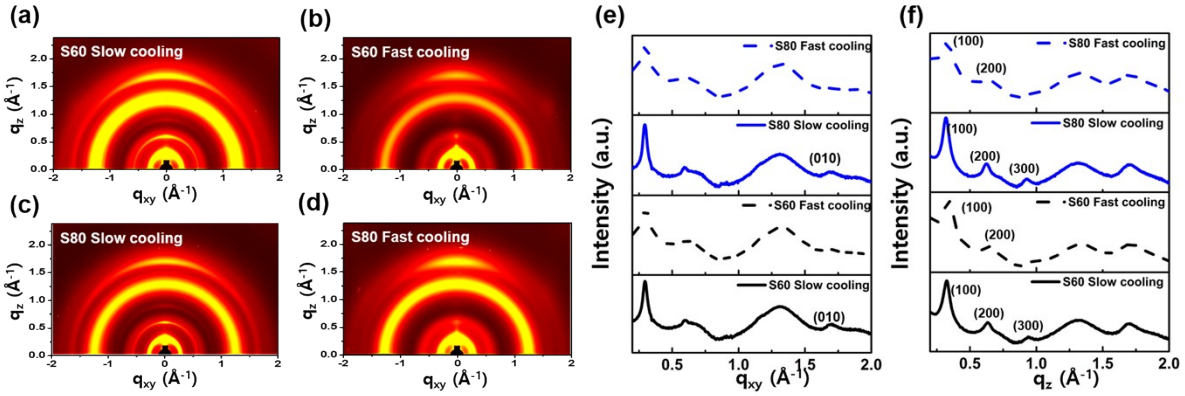

Figure S9. (a-d) Two-dimensional GIWAXS images and (e-f) corresponding line-cut profiles for films coated at H80-S60 and H80-S80 conditions.

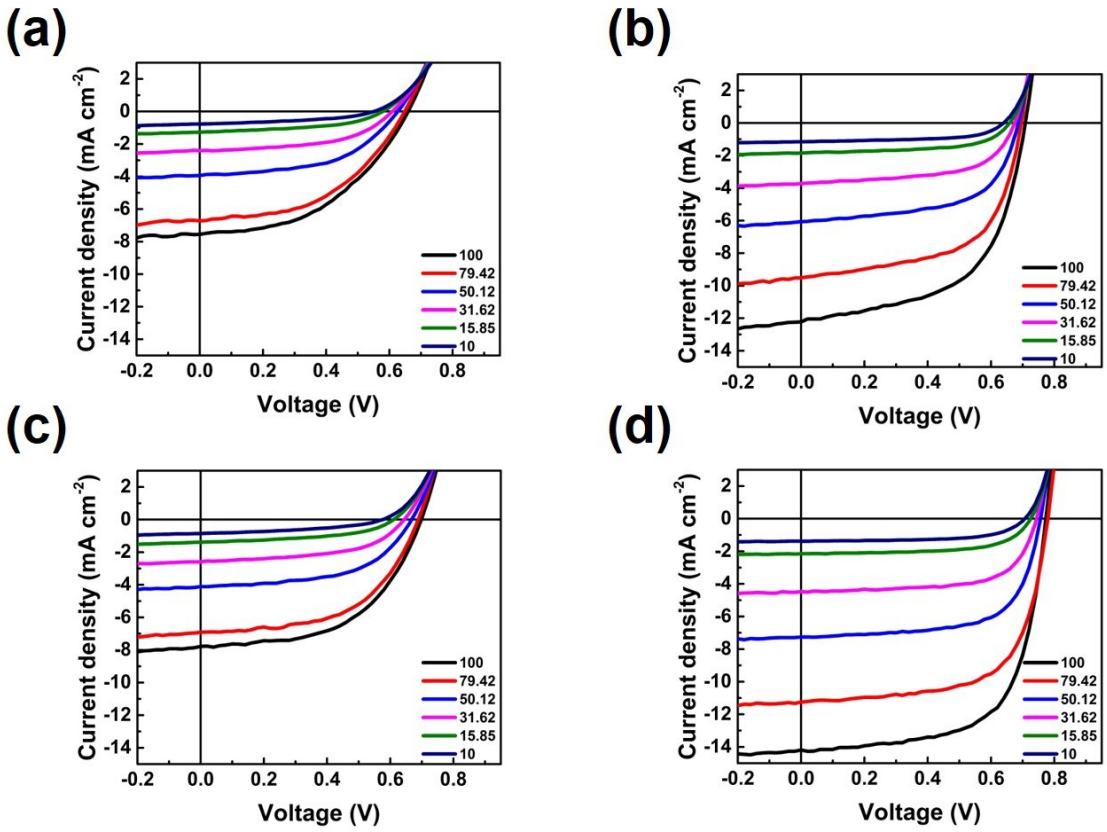

Figure S10. *J-V* curves for each PSC (H25-S25, H25-S80, H80-S25, H80-S80) at variable light intensities.

Table S6. Photovoltaic parameters of devices fabricated by slot die-based all solution process including ETL, active layer and HTL.

Slot die coating condition	HTL	Coating method	J_{SC} (mA cm^{-2})	*Cal.*J_{SC} (mA cm^{-2})	V_{OC} (V)	FF	PCE (%)
H80-S80	AI4083:IPA (1:3)	Spin	9.27	9.41	0.56	0.45	2.31
	PH:IPA (1:3)	Spin	9.79	9.09	0.59	0.44	2.53
	N-PEDOT:PSS : IPA (1:3)	Spin	10.37	9.76	0.64	0.48	3.18
		Slot die	10.29	9.93	0.80	0.60	4.94

Devices were fabricated on glass substrates in air condition. Electron transport layer (ZnO NPs) and active layer (PPDT2FBT:$PC_{71}BM$) were coated by slot die method, then hole transport layer (PEDOT:PSS) were deposited by spin coating or slot die coating. The spin rate for HTL deposition was 5000rpm for 40s, slot die case was based 5mm/s of coating speed on 50 °C substrate temperature.

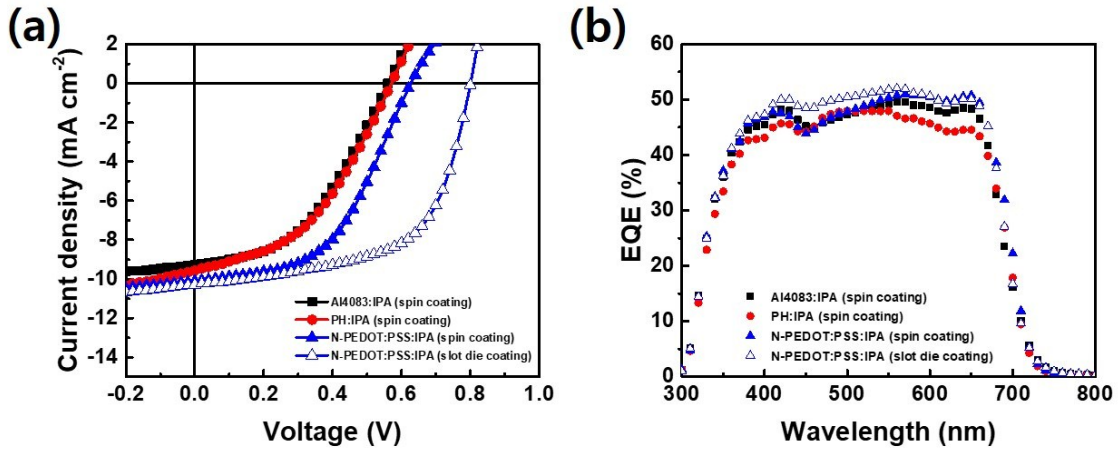

Figure S11. *J-V* characteristics and EQE results of PSCs fabricated by slot die-based all-solution process except electrodes.