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Supporting Information for

A high-throughput flow cytometry-on-CMOS for microwave-frequencies single-cell dielectric spectroscopy

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Fig. S1 The operating principle of the injection-locking on an LC-oscillator. (a) The schematic and (b) the equivalent circuit model of an injection-locked oscillator (ILO) are shown. The feedback with a hard-limiter corresponds to the action of the cross-coupled transistors. Based on the circuit theory, the summation of I_{inj} and I_{osc} must be equal to I_{tank} . (c) Phasor illustrations of the ILO operation are plotted. Two cases are considered. In the first case, the ILO free-running oscillation frequency (ω_{osc}) is equal to the injection frequency (ω_{inj}). Due to on-resonance injection, the LC-resonator contributes zero phase shift, and hence V_{out} is in-phase with I_{inj} . In the second case, the injection frequency is offseted with respect to the ILO oscillation frequency ($\omega_{inj} \neq \omega_{osc}$). Due to off-resonance injection, a phase shift is introduced by the LC-resonator (α) and needs to be compensated by the vector summation of I_{inj} and I_{osc} to ensure stable oscillation. This leads to the rotation of I_{inj} with respect to I_{osc} , creating a phase shift between I_{inj} and $V_{out}(\theta)$. This phase shift is our signal of interest and is measured by the mixer-based phase detector. Comparing with direct measurements on the LC-resonator phase shift (α), amplification in the phase is observed. (d) The effect of reducing the injection strength ($=I_{inj}/I_{osc}$) while the LC resonator is experiencing the same amount of phase perturbation. The weaker the injection strength, the larger the transducer gain. Equations that describe the phase relationship and the ILO sensitivity (S) are shown. Note that Q represents the loaded quality factor of the LCtank. This value is approximately 3 when the electrodes are loaded with water. (e) Simulated ILO transfer curves (output phase versus frequency offset) at different design parameters. For more details, please refer to Chien et. al.¹.



Fig. S2 Chopper stabilization technique for mitigating the 1/f noise from the mixer detector. (a) The application of chopping is performed using binary-phase shift-keying (BPSK) modulation in our interferometry. A chopper is inserted in the upper injection-locking path to periodically swapping the carrier phase by 180°. (b) Since the mixer-based phase detector has an inverted gain at the vicinity of $+90^{\circ}$ and -90° , the chopping converts the desired phase shift. A chopping demodulated signal at the mixer output. The amplitude is proportional to the amount of phase shift. A chopping demodulator is embedded in the baseband transimpedance (TIA) to down-convert the signal back to near-DC. (c) The measured output power spectral density (PSD) shows the effectiveness of the chopping operation. The residual 1/f noise arises from the flicker noise of the ILO₁ and ILO₂, which cannot be alleviated using BPSK chopping.



Fig. S3 Automatic drift calibration and temperature regulation loops. (a) The schematic of the automatic drift calibration loop and the measured sensor output power spectral density (PSD) are plotted. The feedback is performed by first comparing Vout with a fixed reference voltage (Vref), and feeds the filtered error signal to the control voltage of ILO₂ (V_{ctrl}). The sensitivity from V_{ctrl}-to-V_{out} ranges from $20 \sim 40$ (V/V) depends on the injectionstrength. The feedback loop offers a gain of 33, which is set by the ratio of R_4/R_3 (=1M $\Omega/30$ kohm) around the OPAMP (LMC6482, Texas Instrument). This gives an overall loop gain of $56 \sim 62$ dB. The loop filter exhibits a -3dB bandwidth of 0.16 Hz ($R_2 = 1M\Omega$, $C_2 = 1\mu F$). Hence the bandwidth for the automatic drift calibration is at 105 Hz (= 660×0.16 Hz), i.e., drift and offset below 100 Hz will be rejected by the calibration loop. The 105 Hz can be seen at the measured PSD as indicated by the kink around 100 Hz. Note that the FWHM of the measured cell signals is less than 200 µsec. Therefore, high frequency cut-off in the calibration loop does not affect our signal integrity. The noise filter includes $R_1 = 10k\Omega$ and $C_1 = 100pF$, setting the bandwidth at 159 kHz. (b) The schematic of the temperature regulation loop and the measured closed-loop transient response when changing the desired locking temperature (through changing the reference voltage) are plotted. On-chip diode temperature sensor offers a temperature sensitivity ~ -2mV/°C. The off-chip two-stage amplifier (LMC6482, Texas Instrument) offers a gain of 600 (20×30). It compares the measured V_{BE} from the diode against a fixed reference voltage, and feeds back a control signal to adjust the control voltage of the heater. The heater is implemented using thin-oxide transistors and is powered by a separate supply pin at 1.0V. In addition, the number of transistors that are conducting currents can be selected digitally to extend the operating frequency ranges. Note that the closed-loop transient response is measured without CMOS backside cooling, exhibiting a thermal time constant on the order of 1 sec with CMOS embedded in the epoxy (Epo-Tek 302-3M). Backside microfluidic cooling can significantly reduce the thermal time constant by 10×. We estimate the chip is nominally operated at about 39°C from the diode transfer function. On the other hand, the cells are measured at room temperature. This is because the heating of the cells from the chip is minimal due to fast flow rate.



Fig. S4 Measurement setup. (a) The CMOS/microfluidics PCB interfaces with the motherboard with a ribbon cable. The mother board includes (1) multiple low-dropout regulators (LDO), (2) voltage digital-to-analog converters (DACs), (3) level shifters to convert the FPGA control signals from 3.3V to 1.0V, (4) a comparator for frequency calibration, (5) components for the temperature regulation feedback loop, (6) the components for the automatic offset/drift cancellation loop, (7) biasing, and (8) 640 MHz clock generation. (b) The photo of the setup. During the measurements, the daughter board is placed under a microscope. Faraday cage has not been used in our measurements.



Fig. S5 Electrode aging due to electrolysis and potential remedy. (a) A photograph of the uncoated CMOS electrodes after 5 days of measurements in BSA solutions is shown. (b) A photograph of the uncoated CMOS electrodes after 5 days of measurements in BSA solutions is shown. The electrodes are ruptured due to electrolysis. The process of electrolysis can be seen under the microscope with air bubbles and red spots due to aluminum oxidation. (c) A zoom-in view of the electrodes, showing that the aluminum (bright color) has completely disappeared. The remaining parts are the copper (dark green). (d) The biasing on the electrodes, which causes electrolysis, can be potentially removed by AC coupling the electric fields to the electrodes using DC blocking capacitors, C_b . As the equivalent capacitance of the electrodes are 25 ~ 30 fF, a 500 fF of DC blocking capacitors is sufficient without significantly degrading the sensitivity. Such a DC blocking capacitance can either be implemented by coating the CMOS surface with silicon nitride (Si₃N₄) at tens of nm thickness, as discussed in the manuscript, or using coaxial-like electrode configuration where M7 and M9//AP layers enclose the electrode M8. The latter is implemented in the two dummy sensing channels and its effectiveness in electrode protection is verified. (e) Another potential solution other than silicon nitride coating is to replace the aluminum with more inert material, such as gold. This can be achieved using electrodeless nickel immersion gold (ENIG) process.



Fig. S6 Chip photo indicating the removal of silicon nitride using reactive ion etching (RIE). (a) Chip photo. Arrows are pointing to the edge of silicon nitride after RIE. The CMOS electrodes are protected using a slab of PDMS. (b) Zoom-in plot.



Fig. S7 The device photo after epoxy molding for surface leveling. (a) Front and (b) back sides of PCB after epoxy injection. (c) After wire bonding.



Fig. S8 Microfluidics master mold. (a) The photo of 3-D printed master mold. (b) Mold 3-D layout using HFSS (Ansys Inc.). (c) Zoom-in at the 3-D hydrodynamic focusing area.



Fig. S9 Device photo showing the effectiveness of bleach-cleaning protocol. (a) Before and (b) after 20 minutes of bleach cleaning. The protein layer that covers the electrodes is completely removed.



Fig. S10 System calibration flow. It includes: (1) foreground electronics calibration, (2) background reference beads calibration, and (3) reference liquid calibration for the extraction of the permittivity of the culture medium.

a "Electronics calibration" calibrates:

- (1) Frequency mismatch betwee ILO1, ILO2, and QVCO;
- (2) Sensitivity mismatch in oscillator-sensor under injection-locking;
- (3) Non-linearity in the sensor transfer curve;
- (4) Electrode sensitivity (inside the CMOS chip).



Fig. S11 Electronics calibration procedure. (a) The purposes of the calibration are listed. All the calibration steps are performed with the electrodes immersed in the liquid. (b) The schematic shows how the frequency mismatch among ILO1, ILO2, and the QVCO are calibrated. First, the frequencies are adjusted by tuning the frequency control voltages (Vctrl1, Vctrl2, and Vctrl) using digital-to-analog converter (DAC). The frequency mismatch between every two oscillators, i.e. ILO1 and ILO2, is then measured by monitoring their frequency difference (fosc1 – fosc2), using the same mixer detector. The calibration ends when such a frequency has been shifted to DC. When calibrating ILO1 and ILO2, QVCO is turned-off. (c) An illustration of the sensitivity curves is presented. These curves are measured by sweeping the Vctrl1 of ILO1 for the introduction of the known frequency perturbation. The upper row exhibits the transfer curve whereas the lower row shows the derivatives (the sensitivity). It is clearly seen that the sensitivity is different among all four channels. This information allows us to compensate and equalize their

sensitivities during post-processing. The right figure shows the nonlinearity correction in the transfer curve. A *tanh* function is used for curve fitting, and an *inverse tanh* function is used for the correction on the measured cell data. (d) The schematic of the sensing oscillator and the illustration of on-chip switched-capacitors for electrode sensitivity calibration is shown. The right figure shows the measured waveform when enabling the toggling those capacitors. The estimated capacitance is 20aF each.



Fig. S12 In-flow background calibration procedure. (a) Factors that can affect the electrode sensitivity when immersed in the culture medium are listed. (b) The cross-section of the CMOS on-chip electrodes is shown. This figure shows that the electrode sensitivity from the fields fringing downward (into the CMOS dielectric) and upward (into the medium) can be significantly different due to different material composition (SiO₂/silicon versus water medium), its corresponding dielectric constant, and difference in the post-processing and long-term aging. Therefore, electronic calibration alone is insufficient and will lead to inaccurate results. The calibration compensates for such an error by introducing reference material in the medium. (c) The illustration of 3-step background calibrated measurements. First, the beads are characterized accurately, serving as a global reference. Next, cells/beads mixture and cells-only measurements are carried out sequentially for each cell lines. Though the

electrode sensitivity can vary device-to-device and channel-to-channel, cellular data can be accurately extracted through linear scaling using distribution means.



Fig. S13 Reference liquid calibration. (a) The use of calibration curve to infer culture medium permittivity is shown. The calibration curve is best described using 2^{nd} -order polynomial equation. The coefficients (a, b, c) are extracted using standard reference liquids with known permittivity values. These include DI-water, 0.9% saline, and another standard liquid such as ethanol. On the other hand, due to small permittivity difference between DI-water, saline, and the culture medium ($|\Delta \varepsilon| < 2.2$), a 1st-order linear fit with two reference liquids suffices. (b) The microfluidics used in the reference liquid calibration is plotted. The two electrodes are each covered by an independent microfluidic channel. One of the channels is filled with DI-water, serving as reference, and the other is used for injecting different liquids. (c) The measurement setup for the reference liquid measurements is exhibited. Liquid control is performed using syrings and tube clamps. (d) A measurement example from 6 GHz sensing channel. Each liquid is measured three times and the mean is used to extract the permittivity of the cells. (e) The measured culture medium permittivity is plotted with DI-water and 0.9% saline.



Fig. S14 Measured absolute capacitance distribution with 5.8- μ m polystyrene beads. The distribution across all four channel matches to the expected volumetric coefficient of variation (CV) provided by Polyscience Inc. (diameter: mean \pm std = 5.801 μ m + 0.447 μ m). The flow rate in this particular experiment is different from the actual cells/beads measurements.



Fig. S15 Data captured from 6- and 10-µm beads mixture.

		Mean (µm)	Medium (µm)	Standard Deviation (µm)
Human Leukemia	THP-1	13.9	13.57	1.855
	K-562	14.9	14.84	1.9
Breast Cells	MCF-10A	14.8	14.46	2.25
	MDA-MB-231	16.46	16.49	1.83

Table S1. Measured cell diameters using Beckman Z2 Coulter Counter.

 Table S2. Bleach-cleaning protocol repeatability verification using 10-μm polystyrene beads in cell culture medium (raw data, without reference adjustment).

	30-GHz Channel	17-GHz Channel	11-GHz Channel	6-GHz Channel
1 st meas. (aF)	68.0872	82.3352	84.747	91.5149
2 nd meas. (aF)	67.7367	81.9081	83.0299	89.7429
Difference (%)	0.516	0.520	2.047	1.955

Reference:

1. J.-C. Chien, A. M. Niknejad, IEEE J. of Solid-State Circuits, 2016, 51(2), 457.