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Single-crystalline Integrated 4*H*-SiC Nanochannel Array Electrode: toward High-performance Capacitive Energy Storage for Robust Wide-temperature Operation

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Experimental Section

Preparation of integrated SiC NCAs electrode

The single-crystalline 4*H*-SiC wafers were 350 μm in thickness with a crystallographic orientation of exposed {1010} plane and a N doping concentration of 9.8 *at.*%, which are commercially available. The SiC wafers were cut into sheets of 0.7 × 1.5 cm^2, and washed by ultrasonic treatments successively in acetone, ethanol and deionized water. Then they were immersed into a diluted HF solution (the volume ratio of 40 % HF:99 % C_2H_5OH = 1:1) for 2 min to clear the oxides on the surface. In a typical procedure, the SiC sheet and graphite wafer (2 cm × 4 cm) were utilized as the anode and cathode, respectively. A two-stepped procedure was designed to prepare integrated SiC nanoarrays based on an electrochemical anodic oxidation technique at RT. In the first step, the etching medium was set in NH_4HF saturated solution. The pulsed voltage applied was kept constant at 18 V with a cycle time (T) of 0.8 ms and a pause time (T_{off}) of 0.4 ms. The total anodizing time was fixed at 1 min. At the second step, the SiC wafer was oxidized in another etching solution for 5 min at RT, which was composed of HF (40% purity), C_2H_5OH (99% purity) and H_2O_2 (30% purity) with a volume ratio of HF:C_2H_5OH:H_2O_2 = 3:6:1. The applied current kept constant at 120 mA with a cycle time (T) of 0.8 ms and a pause time (T_{off}) of 0.4 ms.

The growth mechnism of SiC NCAs

The etching of SiC *via* anodic oxidation can be divided into two main steps. One is the generation of SiO_2 and the other is the dissolution of the formed SiO_2, which are expressed as bellow:

$$SiC + 2H_2O+4H^+ +2O^- \rightarrow SiO_2 +CO_2 +4H^+ \quad (1)$$

$$SiO_2 + 6HF \rightarrow H_2SiF_6 +2H_2O \quad (2)$$

Firstly, the surface of the SiC anode sheet is partially converted into SiO_2 in the HF solution with the release of CO_2 via reaction (1), once the pulsed voltage is applied. Secondly, the formed SiO_2 will further react with HF *via* reaction (2), making the resolution of SiO_2. The repeated reactions (1) and (2) will cause the continuous resolution of SiO_2, resulting in the etching of SiC with the formed nanoholes within the SiC wafer.

Structural characterizations and electrochemical measurements

Field emission scanning electron microscopy (FESEM, S-4800, Hitachi, Japan) and high-resolution transmission electron microscopy (HRTEM, JEM-2100F, JEOL, Japan) were used for the microstructural characterization of as-fabricated SiC NCAs. The surface species and chemical states were measured by X-ray photoelectron spectroscopy (XPS, ES-CALAB 250Xi, Thermo Fisher Scientific, America). X-ray diffraction (XRD, RINT2000 V/PC, Bruker DS, Germany) was used to investigate the phase compositions.

The electrochemical measurements of the as-fabricated SiC NCAs were performed at RT in a three-electrode configuration with a platinum counter electrode and a Ag/AgCl reference electrode in 2.0 M KCl solution. The single-crystalline integrated SiC NCAs were directly applied as the working electrode, without the use of any additives such as foreign binder or current collector. The cyclic voltammetry (CV), galvanostatic charging/discharging (GCD) and electrochemical impedance spectroscopy (EIS) of the SiC NCAs were investigated on an electrochemical station (Autolab PGSTAT302N, Switzerlands) with a chamber for programming temperature control (ECT100LC, EDESON, China). The specific capacitance was calculated from CV curves according to the following equation:

$$C = \frac{1}{v \times V} \int_{-0.1}^{0.7} i(V) \mathrm{d}V$$

where i is the current response, v is the scan rate, and V corresponds to the voltage range. The specific capacitance was also calculated from GCD plots using:

$$C = \frac{i}{(-dV/dt)}$$

where dV/dt is the slope of the discharge curve.

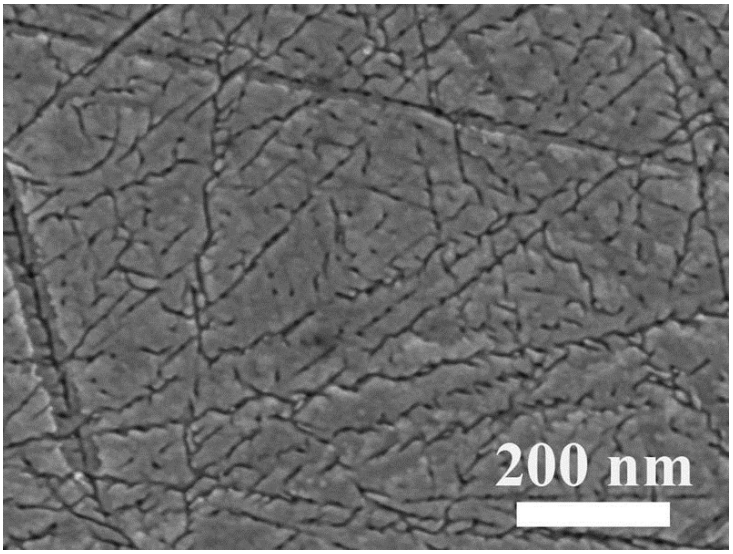

Figure S1. Typical top-view SEM images for the often growth of cap layer during the growth of SiC nanoarrays via the electrochemical anodic oxidation technique.

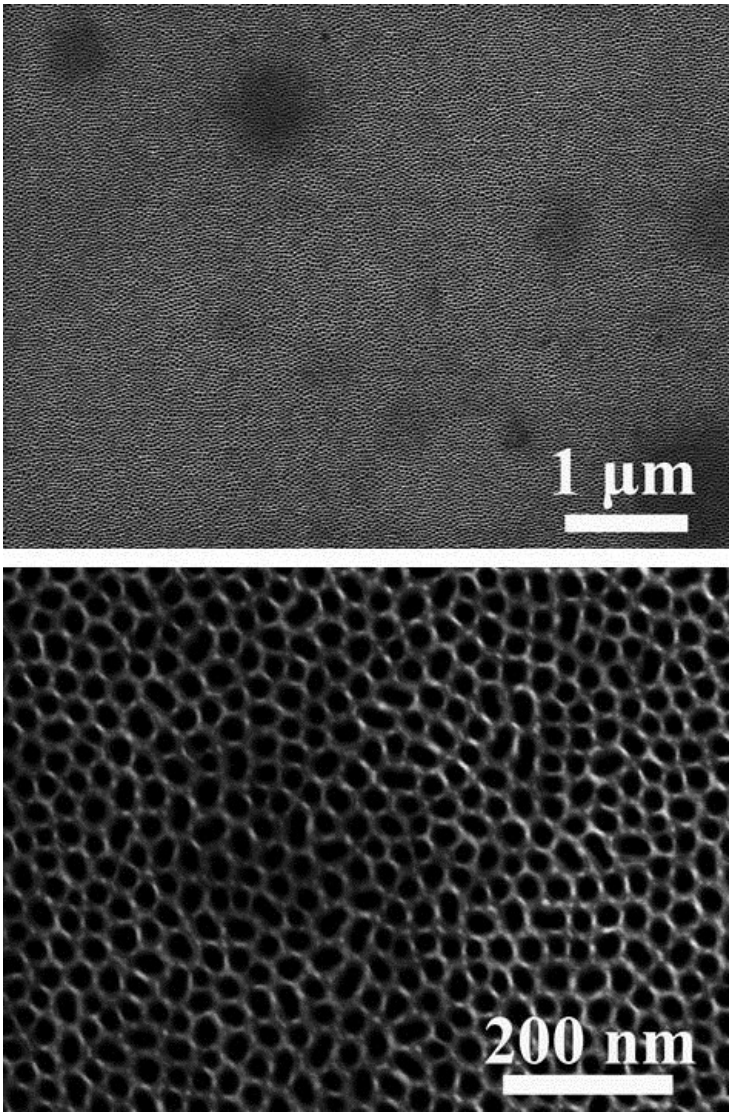

Figure S2. Typical SEM images of the as-fabricated SiC NCAs with fully opened heads under different magnifications.

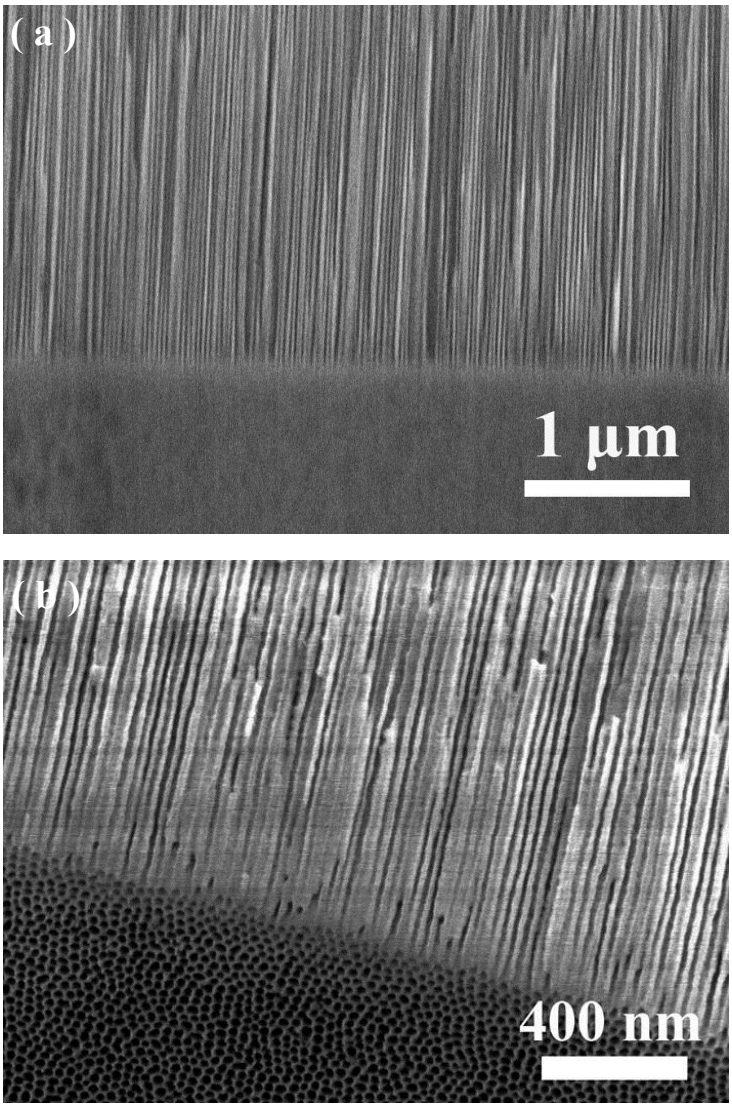

Figure S3. (a) Typical cross-sectional SEM image of the as-fabricated SiC NCAs. (b) Typical cross-sectional SEM image of the SiC NCA electrode after 10000 cycle test.

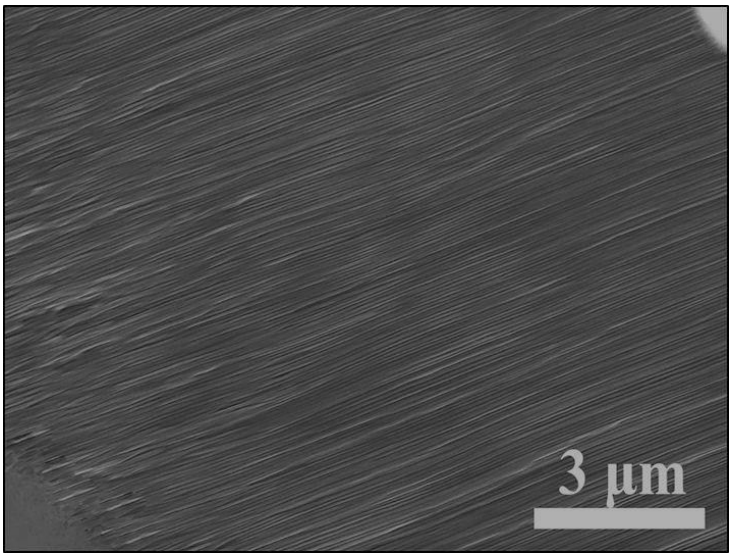

Figure S4. Typical cross-sectional SEM image of the SiC NCAs under a low magnification.

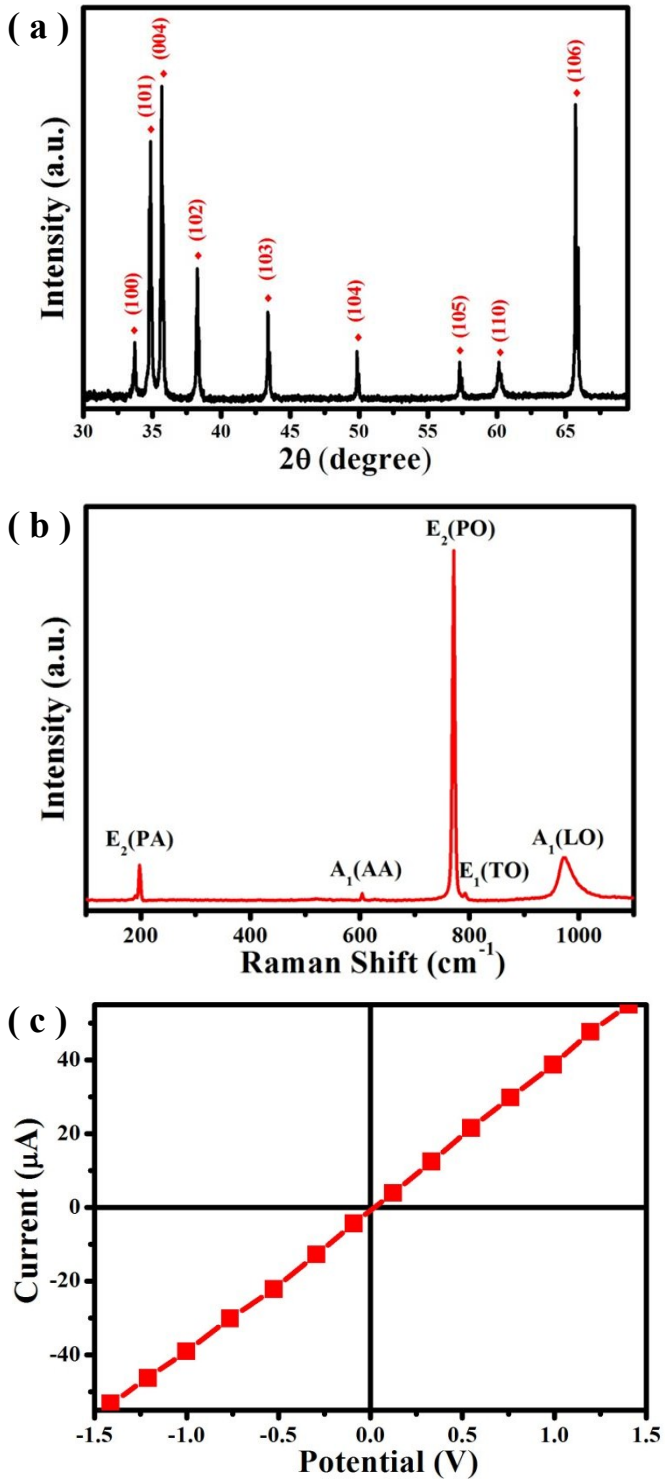

Figure S5. (a) Typical XRD pattern of the SiC NCAs. (b) Typical Raman spectrum of the SiC NCAs under 514.5 nm laser light at room temperature. The peak at 203.5 cm^{-1} is an E_2 planar or transverse acoustic (TA) mode. The peak at 610.5 cm^{-1} is A_1 axial or longitudinal acoustic (LA). The peak at 777.0 cm^{-1} is E_2 planar optical. The peak at 797.5 cm^{-1} is an E_1 mode, and that at 967.0 cm^{-1} is A_1(LO). (c) Conductivity characterization of the SiC NCAs.

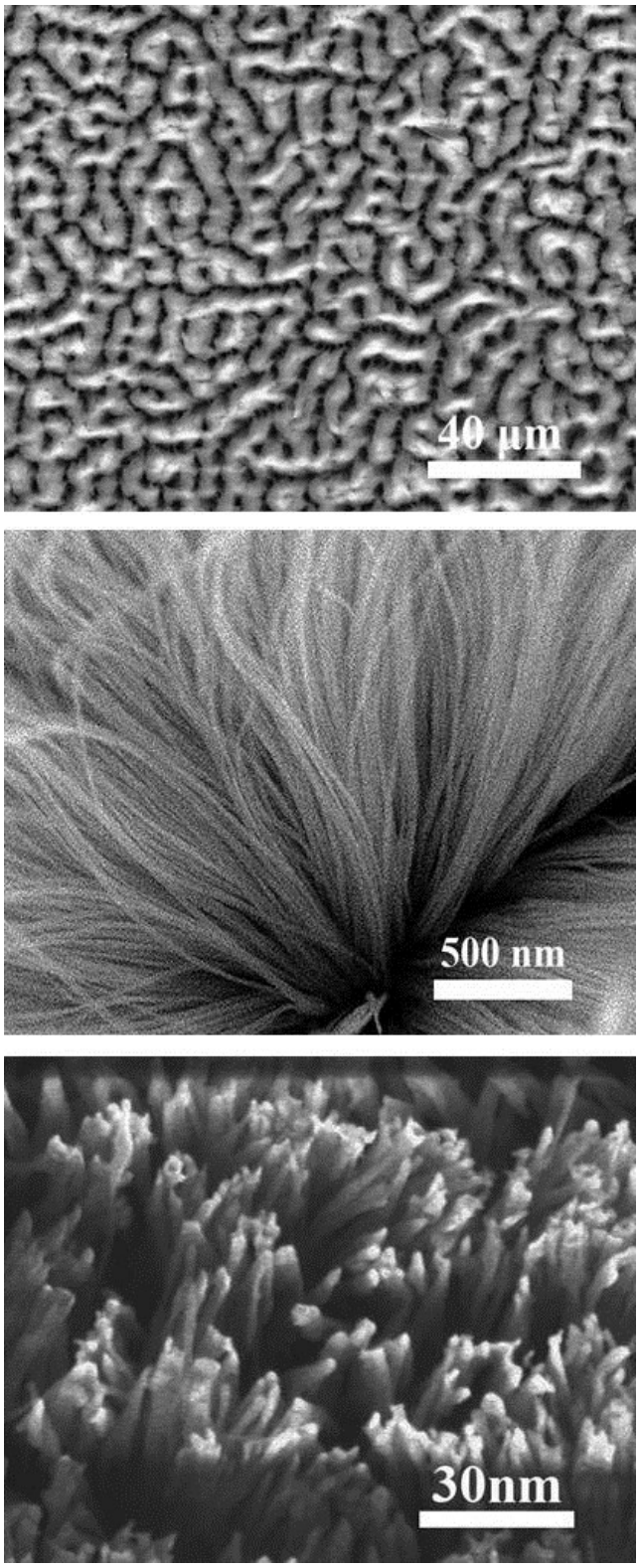

Figure S6. Typical SEM images of the as-prepared SiC nanowire arrays under different magnifications.

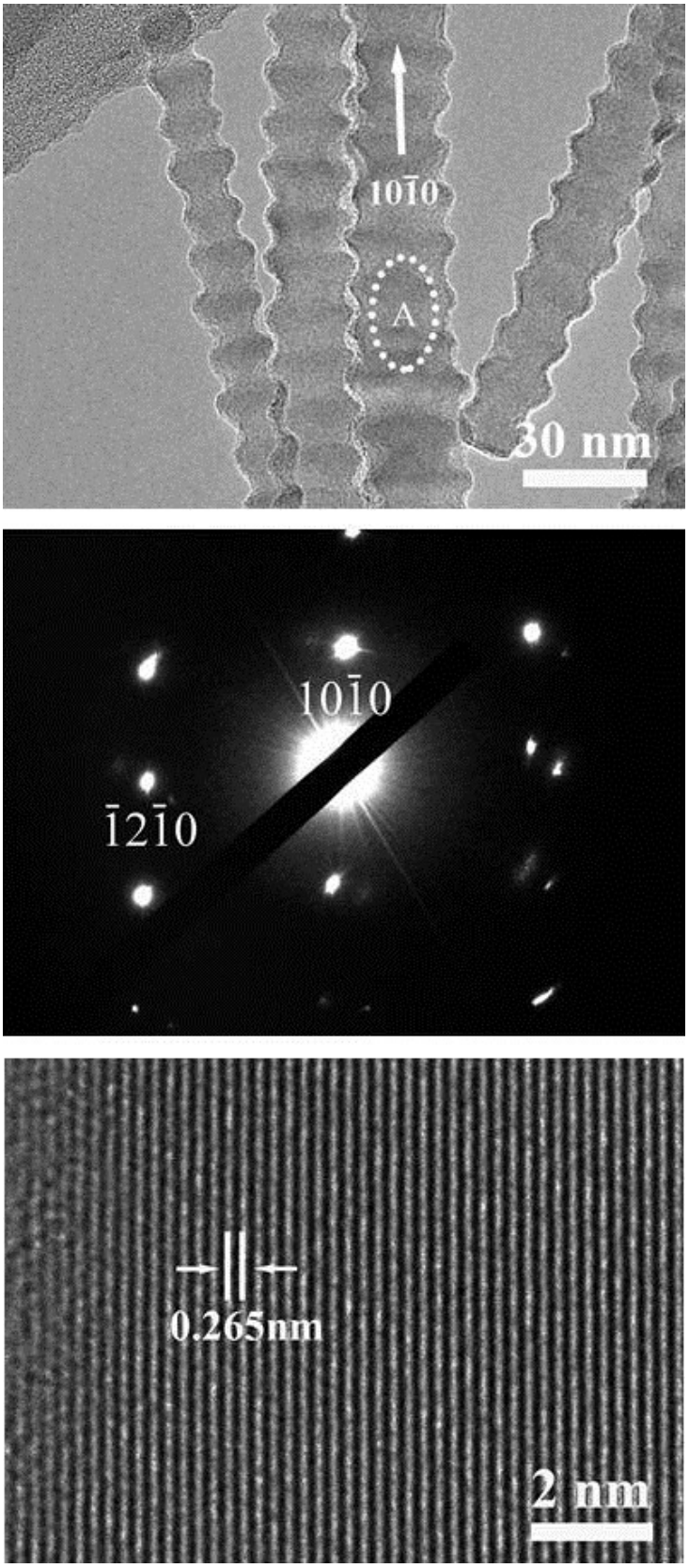

Figure S7. Typical TEM image, SAED pattern and HRTEM image of the as-prepared SiC nanowire arrays.

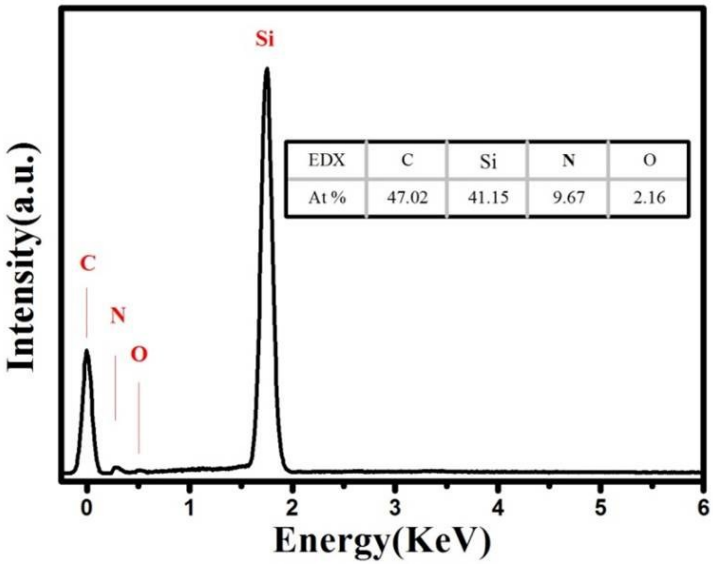

Figure S8. Typical EDX spectrum of the as-prepared SiC nanowire arrays (NWAs) under TEM.

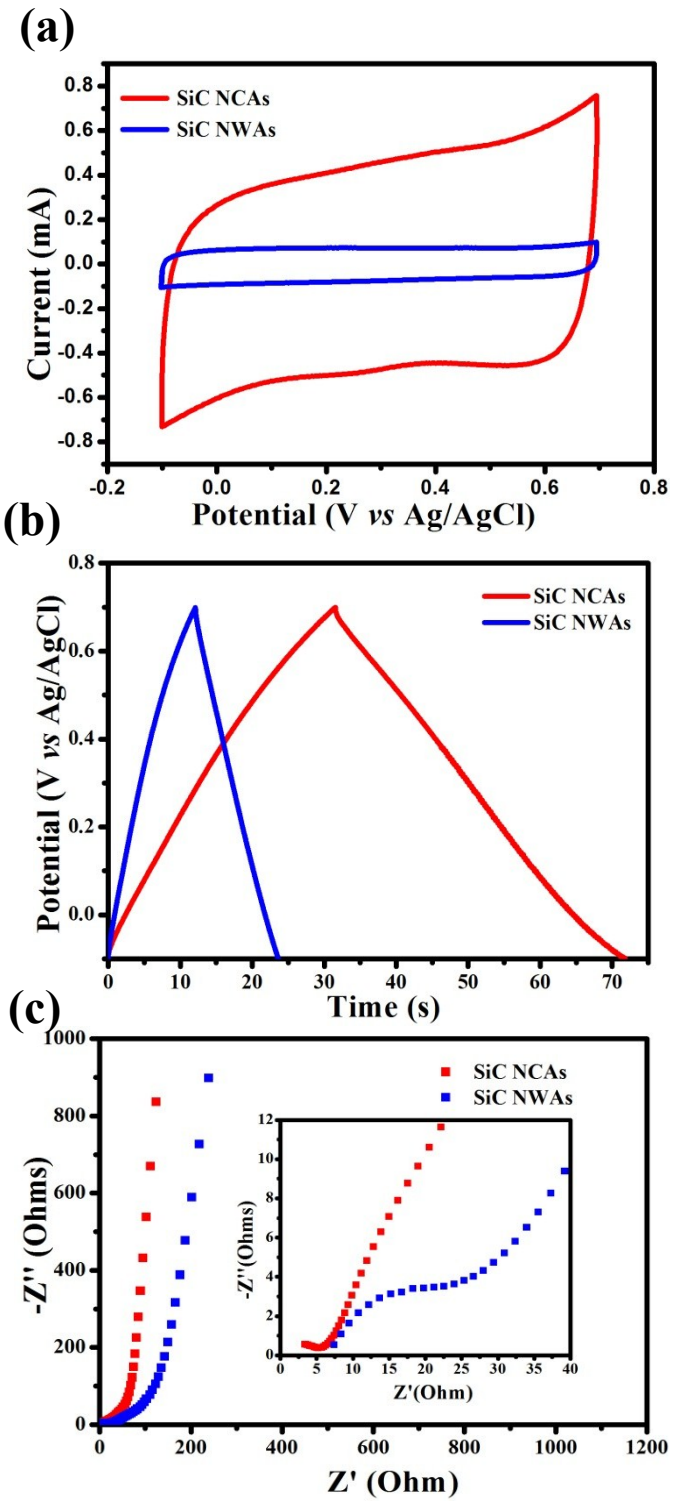

Figure S9. The comparison of electrochemical performances between SiC NCAs and SiC NWAs electrodes.

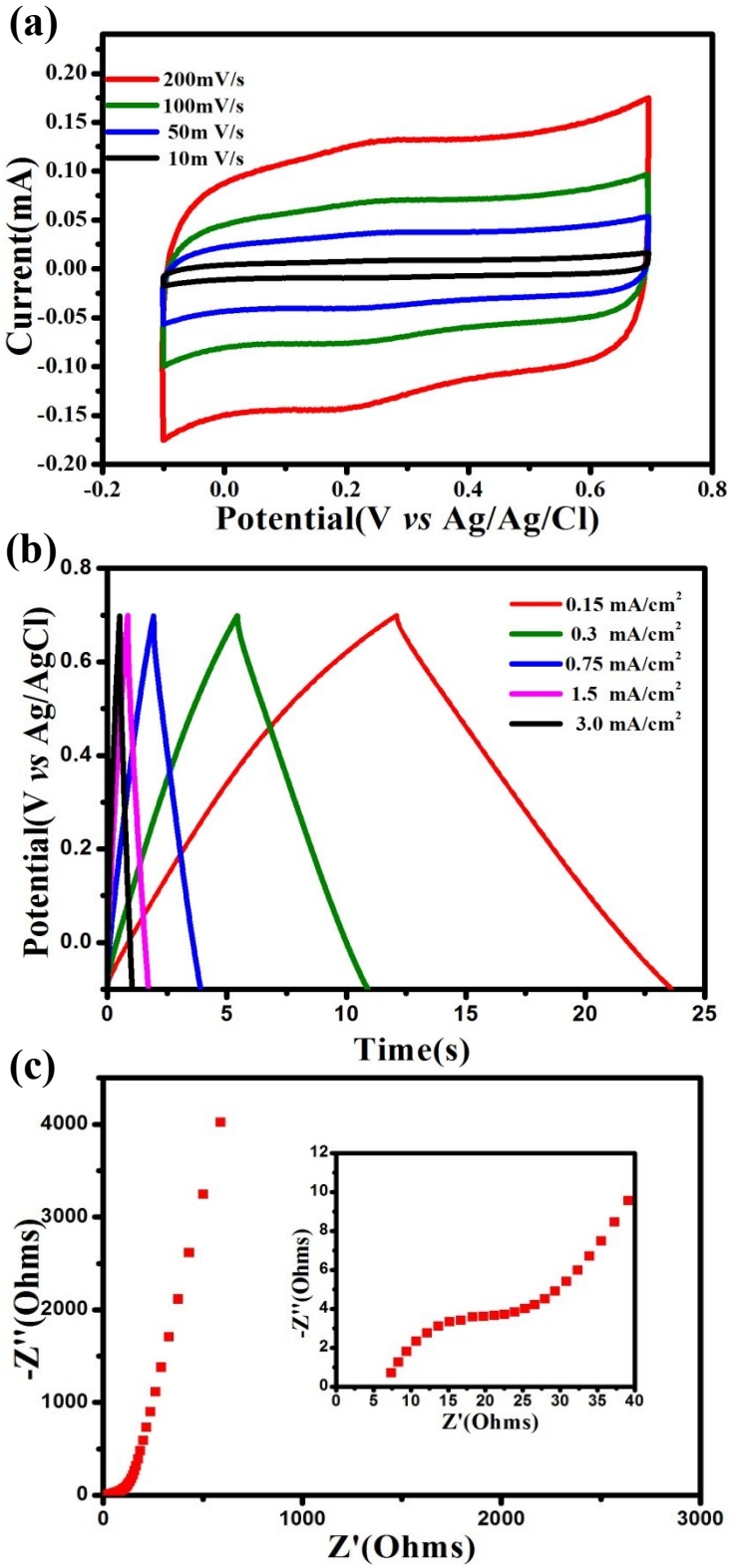

Figure S10. The detailed electrochemical performances of SiC NWAs electrodes.

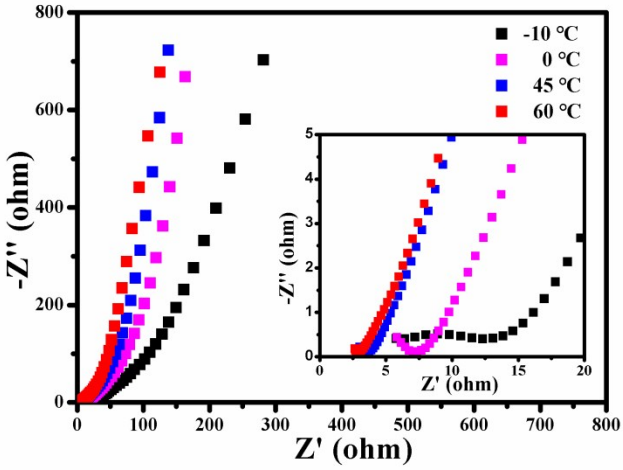

Figure S11. The electrochemical impedance spectroscopy (EIS) of the SiC NCAs electrode under different temperatures.

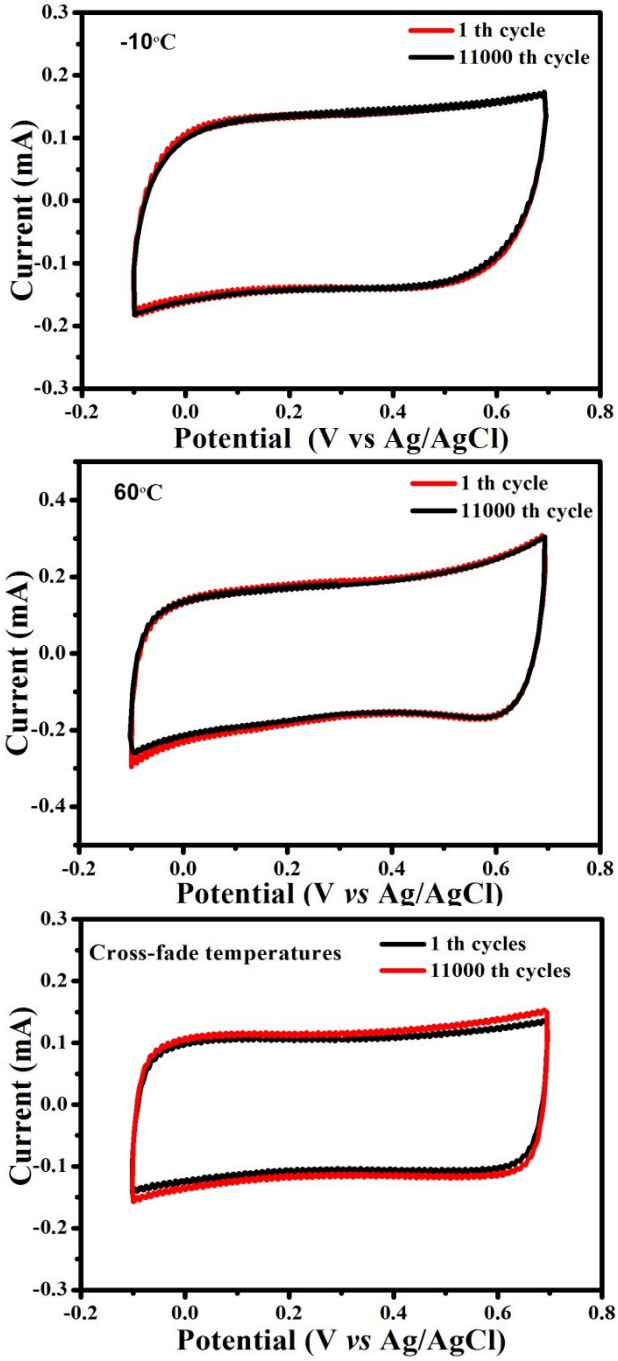

Figure S12. The CV curves of SiC NCAs electrode when subjected to be serviced under low, high and cross-fade temperatures between low and high temperatures for 11000 charge-discharge cycles.

Table S1. Overview of the specific capacitance of SiC array structure

Materials	Synthetic method	Specific capacitance	Stability	Ref.
SiC Nanochannels	Electrochemical anodic oxidation	14.8 mF cm^{-2} at 10mV s^{-1}	Retaining 96% for 10000 cycles	This work
SiC Nanowires array	Chemical vapor deposition	350 μF cm^{-2} at 0.5V s^{-1}	Retaining ~100% for 2000 cycles	1
SiC Nanowires	Low-pressure chemical vapor deposition	240μFcm^{-2} at 100mV s^{-1}	Retaining 95% for 200000 cycles	2
SiC Nanowires	Chemical vapor deposition	23mF cm^{-2} at 50 mV s^{-1}	Retaining 90% for 100000 cycles	3
SiC Nanowires	Chemical vapor deposition	4.7mF cm^{-2} at 10mV s^{-1}	Retaining 98% for 10000 cycles	4
Si/SiC Nanowires	Etch technique/chemical vapor deposition	1.7mF cm^{-2} at 50 mV s^{-1}	Retaining 95% for 200000 cycles	5
SiC nanowires	Carbothermal reduction method	37 mF cm^{-2} at 0.3 A cm^{-2}	Retaining 100% for 2000 cycles	6
SiC Nanowires	Chemical vapor deposition	92 μFcm^{-2} at 100mVs^{-1}	Retaining 60% for 10000 cycles	7

Table S2. Overview of the specific capacitance of SiC array structure

Materials	Electrolyte	Capacitance change	Stability	Ref.
SiC Nanochannels	KCl aqueous solution	136% ,-10 to 60°C	Retaining 97.3%, 96.8 % and 95.5 at -10, 60 °C and cross-fade temperatures between -10 and 60 °C for 11000 cycles, respectively.	This work
TiC nanotube branches	$LiClO_4$ acetonitrile solution	150%,-15 to 65 °C	Retaining 67% at -15 °C for 50000 cycles	8
TiC@crystalline PPy (PVA)	$NaNO_3$ aqueous solution	112%,-18 to 60 °C	Retaining 40% at 60 °C for 5000 cycles	9
Graphene Thin sheet	Li_2SO_4/Ethylene glycol/Water	134,-20 to 45 °C,	Retaining 92% at 45°C for 5000 cycles	10
Carbon	Eutectic mixture of ionic liquids	76% , -50 to 40°C	/	11
$NiCo_2O_4$	KOH aqueous solution	150% , -10 to 60 °C	/	4

Reference:

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