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Supporting information
Complementary MoS_2 fin-shaped field effect transistors

Yann-Wen Lan[1*], Po-Chun Chen[1], Yun-Yan Lin[1], Ming-Yang Li[2], Lain-Jong Li[3], Yu-Ling Tu[2], Fu-Liang Yang[2], Min-Cheng Chen[4], Kai-Shin Li[4*]

[1]Department of Physics, National Taiwan Normal University, Taipei 11677, Taiwan

[2] Research Center for Applied Sciences, Academia Sinica, Taipei, Taiwan.

[3] Physical Sciences and Engineering Division, King Abdullah University of Science and Technology (KAUST), Thuwal, Kingdom of Saudi Arabia.

[4] National Nano Device Laboratories, National Applied Research Laboratories, Hsinchu 30078, Taiwan.

Corresponding authors: Email: ywlanblue@gmail.com; ksli@narlabs.org.tw

Device fabrication

The schematic flow chart for fabrication process is shown in Figure SF1. In the beginning, 30 nm SiO_2 was formed on Si substrate as isolation layer of back gate oxide (BOX). An 80 nm poly-Si film was then prepared by 600°C low-pressure CVD (LPCVD) furnace. After W_{fin} = 30 nm poly-Si fin patterned by using e-beam lithography technology, oxidation process was adapted to oxidize poly-Si surface forming 20 nm SiO_2. Afterwards, by utilizing dry etching, 20 nm SiO_2 on poly-Si source (S) and drain (D) surface which is defined by positive photo resist can be removed for embedded S/D contact, while the undefined region of photo resist serve as a protected layer for the rest of the substrate. The dimension of the S and D electrodes is 60 x 60 um^2. BF_2 and As implantation was performed at S/D doping and then rapid thermal annealing at 950°C was conducted for S/D activation. High quality MoS_2 thin film was grown along S/D edge on the surface of silicon dioxide (SiO_2) fin structure by solid-source CVD process at 755°C. Although the growth of MoS_2 thin film shows the random nucleation behavior, SiO_2 fin structure and S/D first structure provide seed layer function to guide the MoS_2 thin film synthesized and align with channel region between S and D, as shown in Figure SF1(g). Finally, 3 nm SiO_2 interfacial layer and 10 nm HfO_2 high-k dielectric were deposited by atomic layered deposition (ALD) while TaN/TiN was employed for metal gate by physical vapor deposition (PVD) system. Figure SF1(h) and SF1(i) show the device layout and the SEM image of the completed device with top gate structure respectively, where one can realize that the MoS_2 channel length is 100nm while the top gate is overlapped with S/D by an area of about 60000nm^2.

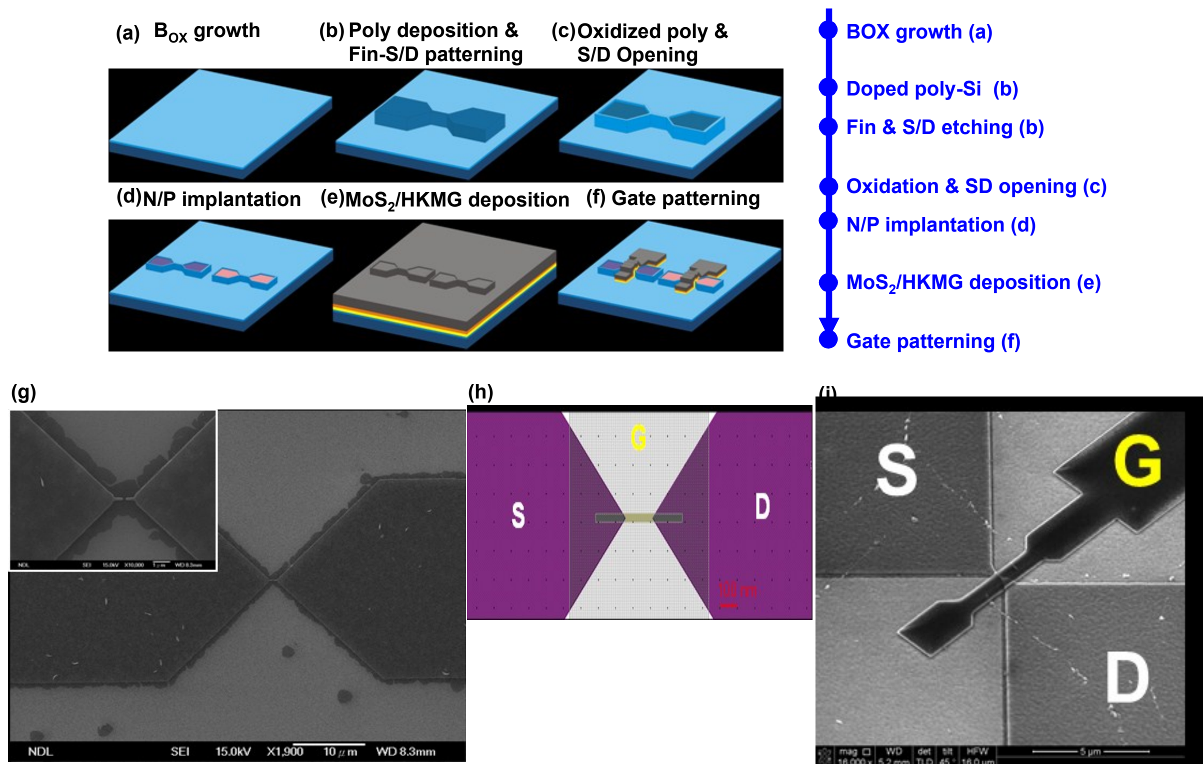

Figure. SF1| (a) ~ (f) Fabrication process scheme. 30 nm SiO_2 grew on Si substrate is followed by polysilicon deposition and fin structure patterning. Soon after full oxidation of poly silicon at fin structure, oxide on source/drain surface is dry etched away until polysilicon exposes where ion implantation with dose 1E15 AsH and BF_3 act respectively as source of N- & P-type. Afterward, MoS_2 grow on the defined substrate with 10nm HfO_2 ALD deposition on top. Subsequently, top gate TaN/TiN is defined by e-beam lithography as well as plasma etching. (g) SEM image of high quality MoS_2 thin film grown on the edge of S/D electrodes (h) Device layout for showing overlap region. (i) SEM image of the completed device with top gate structure.

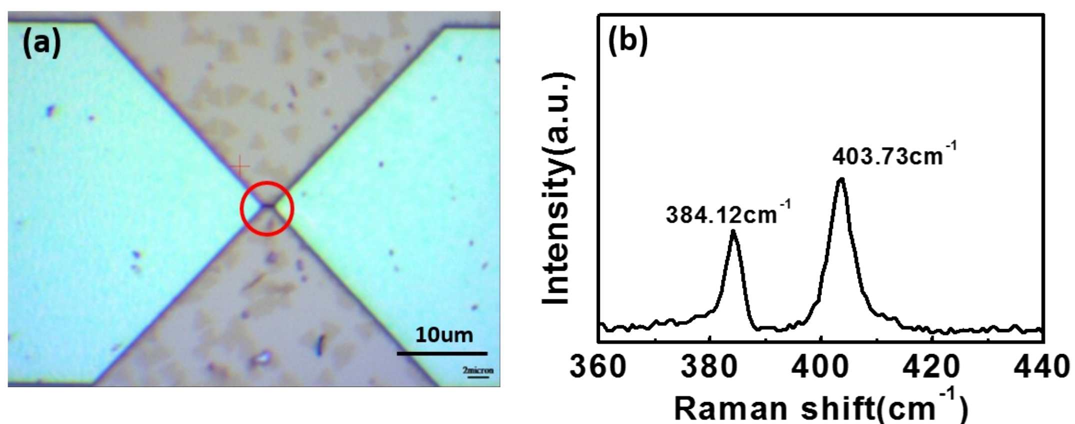

Figure. SF2| (a) Typical optical image of MoS_2 grew on the fin-shaped pattern substrate and (b) its Raman spectrum. The source and drain are blue pads and the dispersed triangle flakes are CVD MoS_2. Raman spectra shows that the separation of A_{1g} and E^1_{2g} ≈ 19.6cm^{-1}, which indicates that the MoS_2 between S and D is a few layers. Red circle marked in (a) is the measured position.

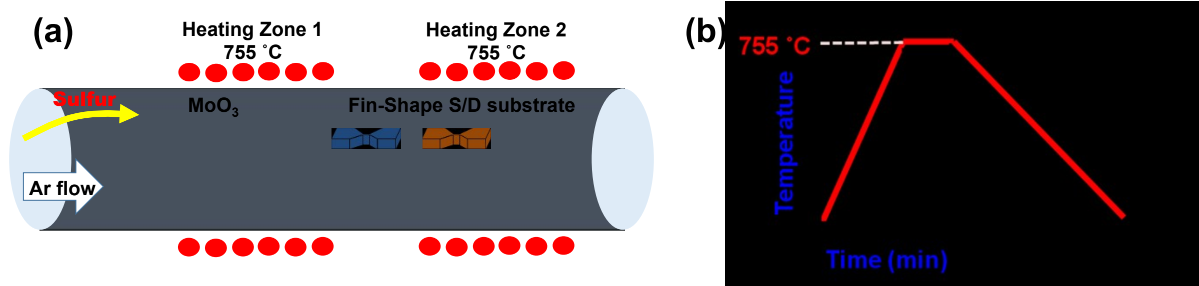

Figure. SF3| Schematic plot of chemical vapor deposition of MoS_2 synthesis. (a) Configuration of CVD set up. (Reprinted from ref. [23], Copyright 2016, with permission from IEEE) (b) Relation between time and temperature during the CVD process.

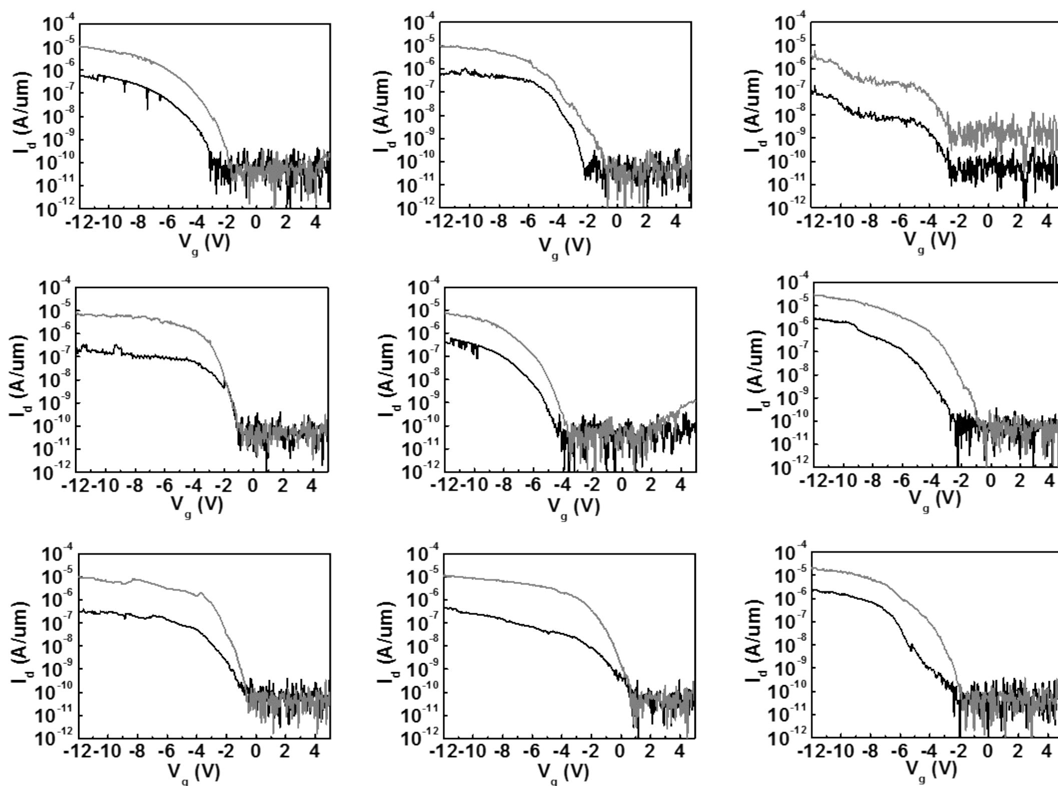

Figure. S4| I_dV_g characteristics of other P-type MoS_2 fin-shaped field effect transistors at V_D=0.1V and 1V.

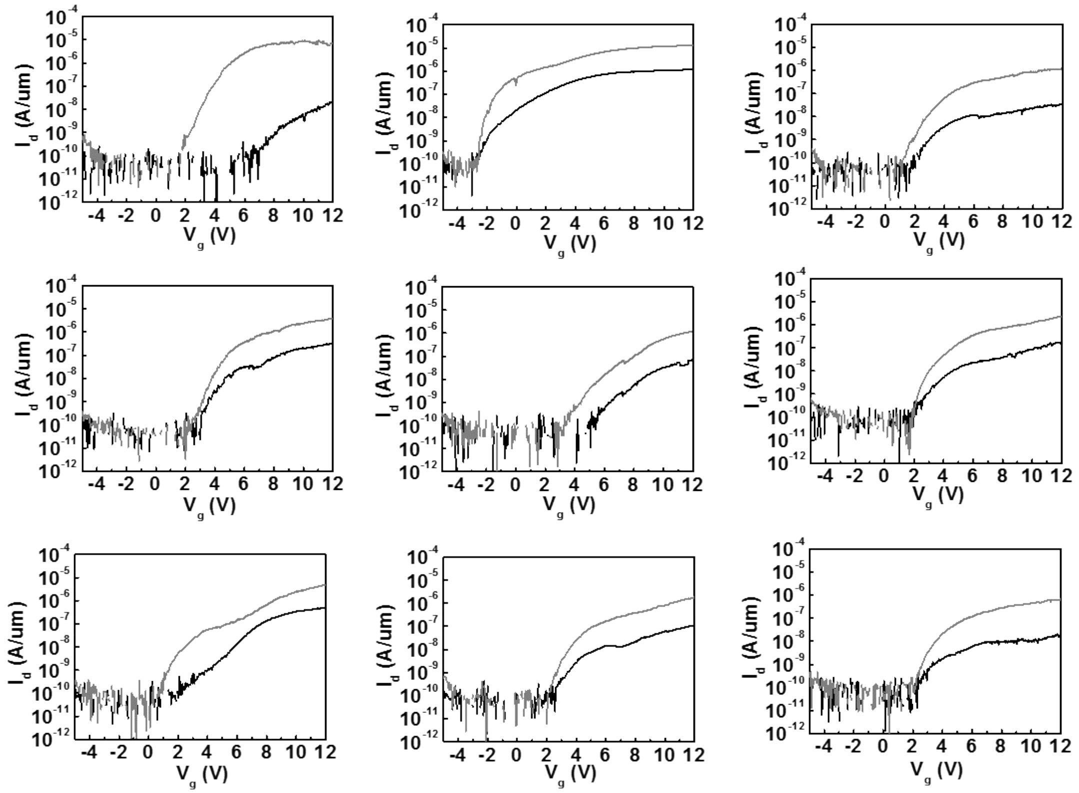

Figure. S5| I_dV_g characteristics of other N-type MoS_2 fin-shaped field effect transistors at V_D=0.1V and 1V.