Electronic Supplementary Material (ESI) for Nanoscale.

Supporting Information

Efficient and reliable surface charge transfer doping of black phosphorus via atomic layer deposited MgO toward high performance complementary circuits

Wugang Liao[1,2,#], *Lin Wang*[1,2,#], *Li Chen*[1,2], *Wei Wei*[1,2], *Zhe Zeng*[1,2], *Xuewei Feng*[1,2], *Li Huang*[1,2], *Wee Chong Tan*[1,2], *Xin Huang*[1,2], *Kah Wee Ang*[1,2,*], *Chunxiang Zhu*[1,2,*]

[1]Department of Electrical and Computer Engineering, National University of Singapore, 4 Engineering Drive 3, 117583 Singapore

[2]Centre for Advanced 2D Materials and Graphene Research Centre, National University of Singapore, 6 Science Drive 2, 117546 Singapore

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# Both authors contributed equally to this work.

*E-mail address: eleakw@nus.edu.sg; elezhucx@nus.edu.sg

1. MgO film deposition by ALD.

MgO is deposited in a Cambridge NanoTech reactor with Bis(Ethylcyclopentadienyl)Magnesium [$(EtCp)_2Mg$] and H_2O as the precursors. Nitrogen (N_2) is used as the purge gas and the carrier gas. The sequence of pulses for one cycle deposition of MgO is H_2O (15 ms)/N_2 (20 s)/ $(EtCp)_2Mg$ (1 s)/N_2 (20 s). The deposition temperature is kept at 150 ^oC. A total of 200 cycles was used for MgO layer deposition, corresponding to the thickness of 25 nm. The overall MgO ALD reaction using $(EtCp)_2Mg$ and H_2O can be written as following: $(EtCp)_2Mg + H_2O \rightarrow MgO + 2HEtCp$.

2. Al_2O_3 deposition by ALD.

Al_2O_3 deposition by ALD: Al_2O_3 is grown in the same reactor using trimethylaluminum (TMA) and H_2O as the precursors. The sequence of pulses in a cycle deposition of Al_2O_3 is TMA (0.015 s)/N_2 (40 s)/H_2O (0.015 s)/N_2 (40 s). The deposition temperature is kept at 120 ^oC. The deposition of 200 and 500 cycles were adopted for the passivation layer and the dielectric layer of Al_2O_3, respectively. And the deposition rate of Al_2O_3 is 0.1 nm/cycle.

3. Stability of MgO doped n-type BP FET.

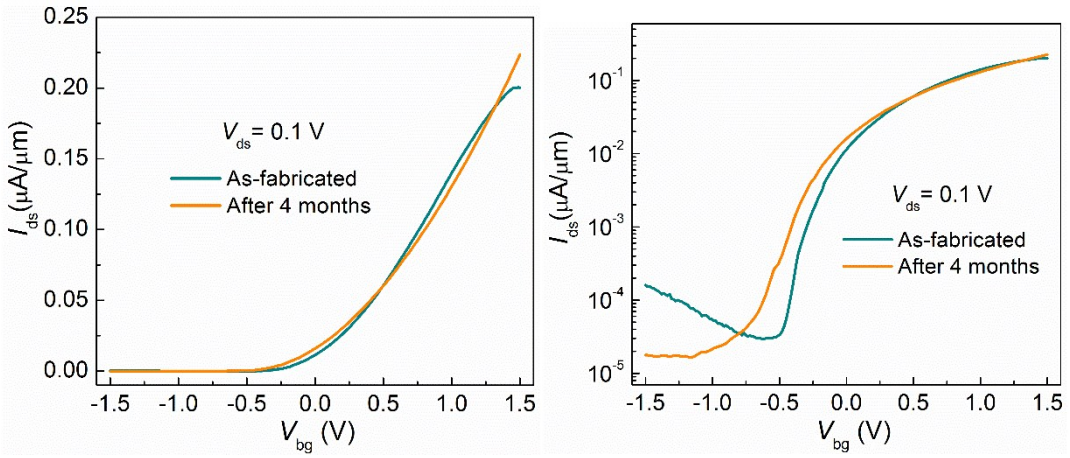

Figure S1. The transfer curves of a MgO doped BP FET on Al_2O_3 (50 nm)/Si substrate as fabricated and after 4 months in linear scale (left) and logarithm scale (right).

4. Extraction of Schottky barrier height.

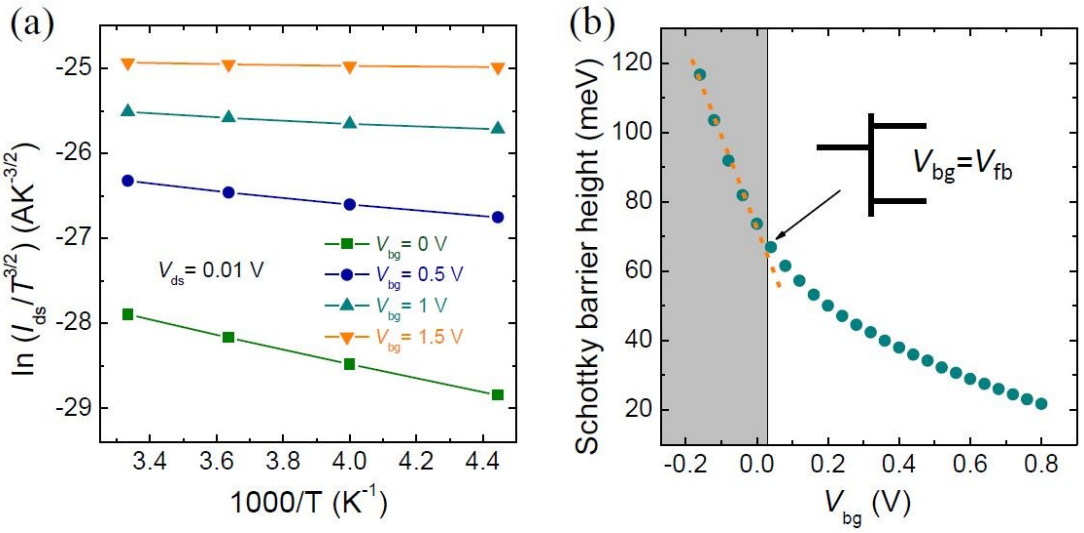

Figure S2. (a) Arrhenius-type plots of ln ($I_{ds}/T/^{3/2}$) against 1000/T at typical gate biases for V_{ds} = 0.01 V. (b) Extracted effective Schottky barrier height in dependence of V_{bg}.

We extract the Schottky barrier height by measuring the transfer properties of the device at various temperatures. In thermionic emission model for 2D systems, the drain-source current (I_{ds}) is related to the Schottky barrier (Φ_{SB}) by the equation I_{ds} = $AA^*T^{3/2}\exp(q\Phi_{SB}/K_BT)$, where T is the temperature, A is the area of the Schottky junction, $A^*= e(8\pi m^*K_B^3)^{1/2}/h^2$ is the 2D equivalent Richardson constant, e is the elementary charge, K_B is the Bolzmann constant, m^* is the effective mass and h is the Planck constant. To extract the barrier height at the BP/matal (Ti) contacts, the Arrhenius-type plots (ln ($I_{ds}/T/^{3/2}$) as a function of 1000/T) is shown in Figure S2a. Further, the electron barrier height is estimated to be ~60 meV (Figure S2b).

5. P-N Homojunction Diode.

The p-n junction is one of the important and fundamental building blocks of the electronics and optoelectronics. BP-based p-n homojunction diode was fabricated by selective doping with 25 nm thick MgO. Figure S3 shows the typical rectification characteristics of a BP homojunction diode.

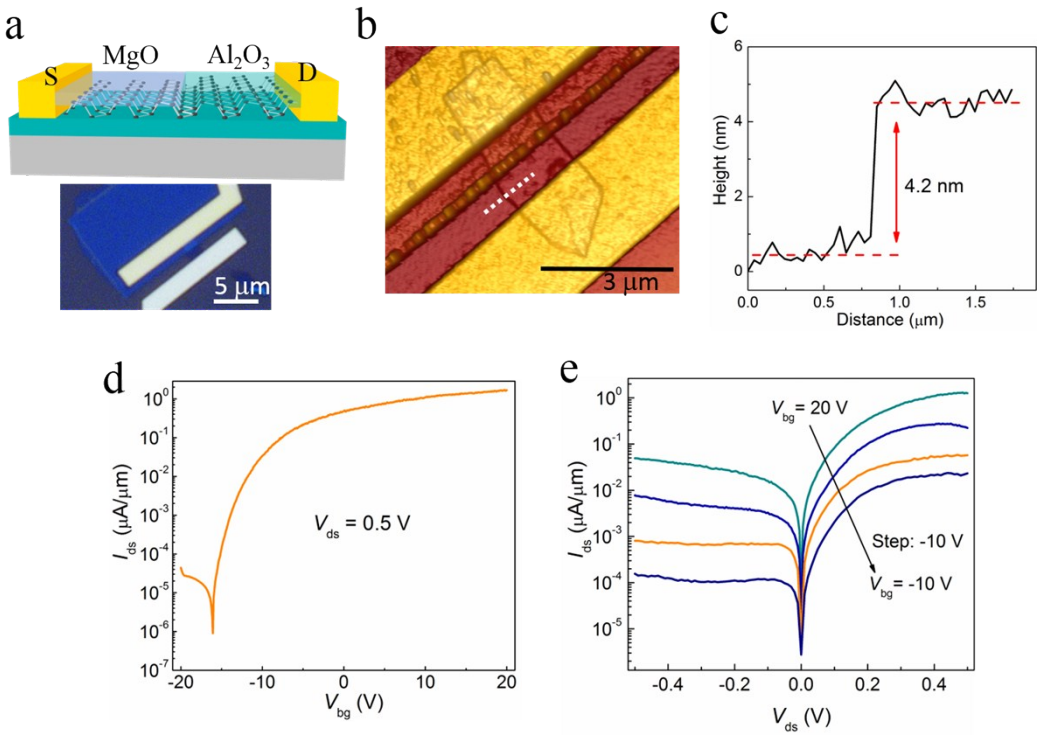

Figure S3. (a) Schematic illustration and optical image of the as-fabricated p-n diode on 90 nm SiO_2. (b) Atomic force microscopy image of the BP diode. (c) The line profile at the flake edge of BP flake indicates a thickness of 4.2 nm (~8 layers). The length and width of the BP channel is 1.65 and 1.55 μm, respectively. (d) The drain current as a function of gate voltage ranging from -20 to 20 V. (e) The drain current as a function of drain voltage of the 4.2 nm BP diode in logarithmic scale with gate voltage range from -10 to 20 V.

6. Gate capacitance measurements.

The dielectric constant (*k*) value of the Al_2O_3 deposited by atomic layer deposition (ALD) was obtained from a metal(Ti/Au)-Al_2O_3-p++ Si capacitor structure. From the capacitance-voltage (C-V) plot shown in Figure S4, the gate capacitance density was measured to be 1.25 × 10^{-7} F/cm^2, and the *k* value of the Al_2O_3 is extracted to be 7.12.

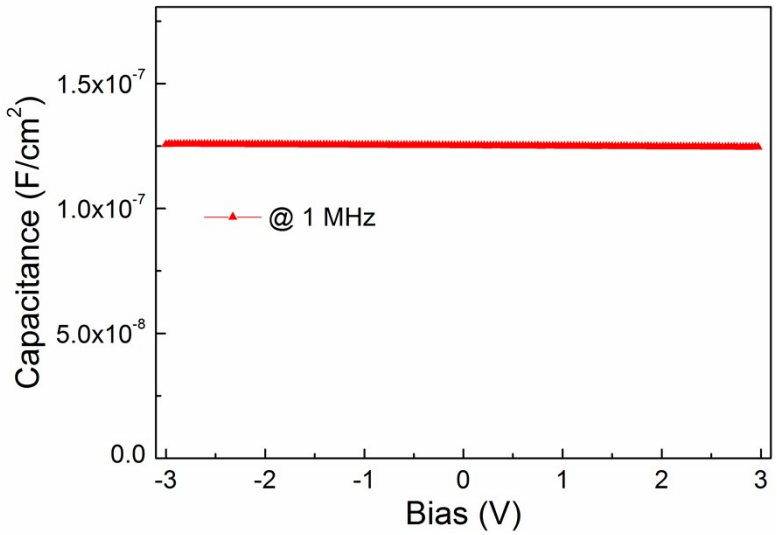

Figure S4. The C-V curve of a metal-Al_2O_3-p^{++} Si capacitor as a function of gate voltage at 1 MHz.

7. Transfer characteristics I_{ds}-V_{bg}.

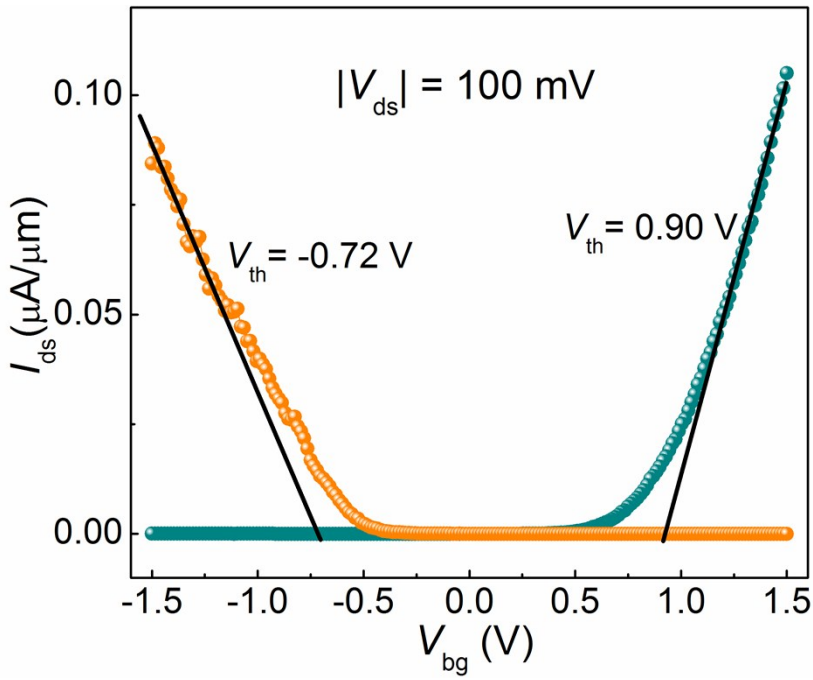

Figure S5. Transfer characteristics I_{ds}-V_{bg} of both p-FET and n-FET in linear scale at $|V_{ds}|$= 100 mV, showing the subthreshold voltage of -0.72 and 0.90 V for the p-FET and n-FET, respectively.

8. Static transfer characteristics of the CMOS BP inverter.

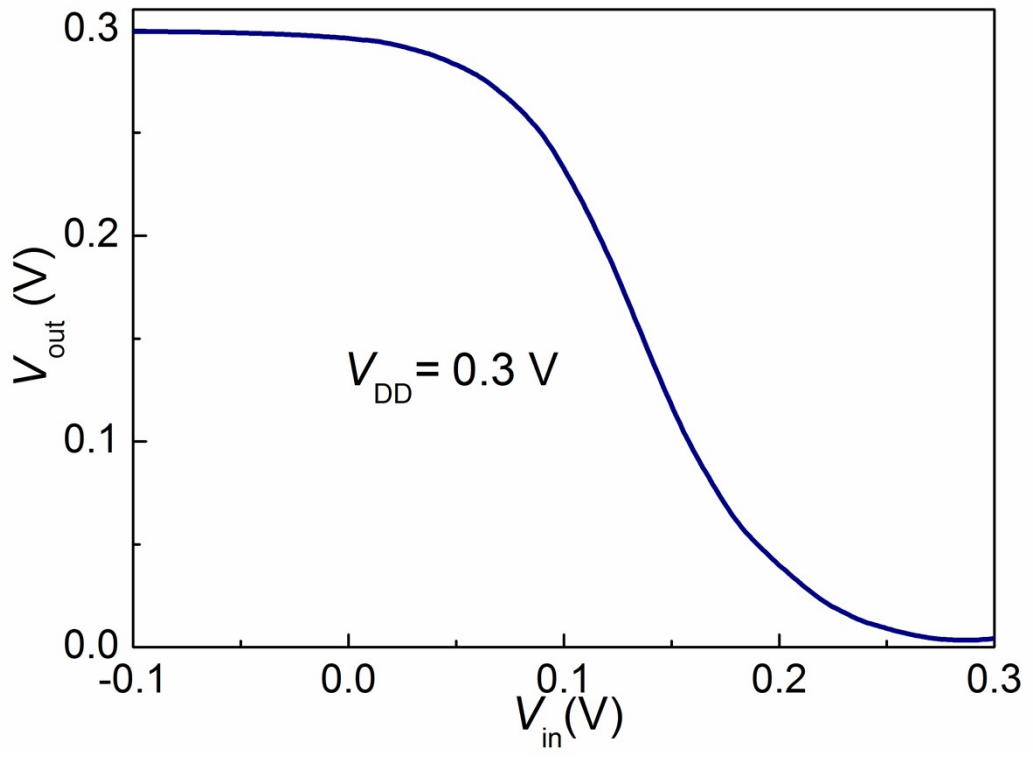

Figure S6. Voltage transfer characteristics of our BP inverter at V_{DD} of 0.3 V.

9. Output voltage dynamics (V_{out}) for our CMOS BP inverter.

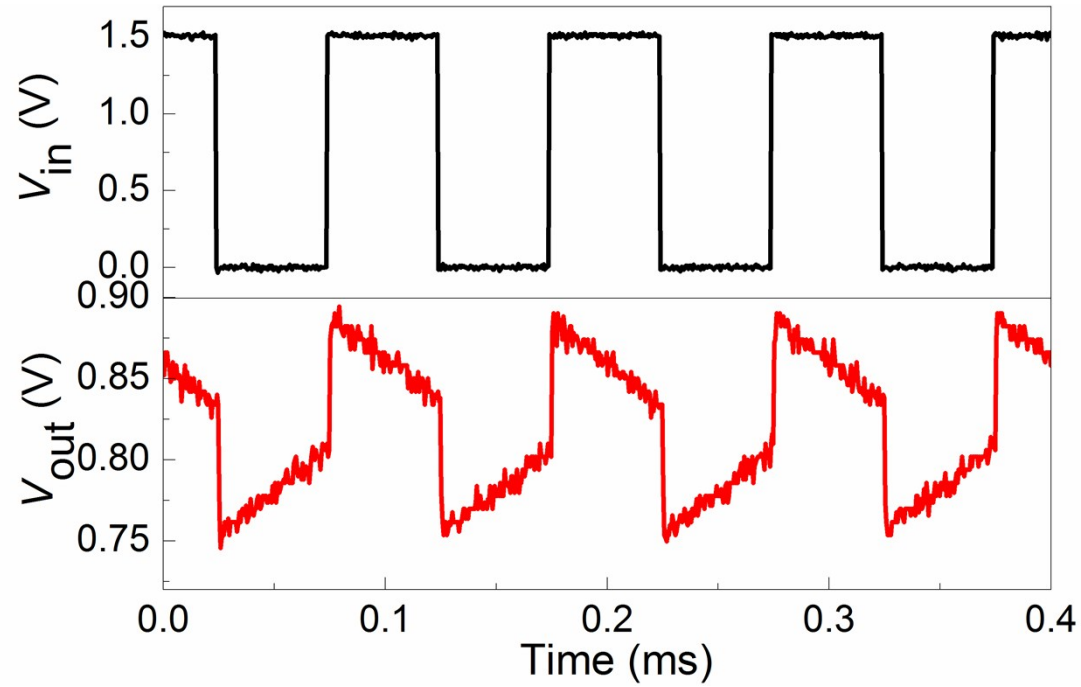

Figure S7. Output voltage dynamics (V_{out}) for our CMOS BP inverter at a supply voltage of 1.5 V under an AC square wave at a frequency of 10 kHz.

10. Intrinsic delay estimation.

The intrinsic delay of the inverter can be estimated as follows. The parasitic capacitance C_p is mainly contributed by the gate capacitance of the two FETs, and can be calculated by $C_p=(L_pW_p+ L_nW_n)\varepsilon_r\varepsilon_0/t_{ox}$, where L is the length of the gate electrode, W is the channel width, ε_r is the dielectric constant of Al_2O_3, t_{ox} is gate dielectric thickness, and ε_0 is the permittivity of free space.

As a result, C_p=0.004 pF is obtained. In addition, from Figure 4d, the peak drive current of the inverter at 1.5 V_{dd} can be obtained as 250 nW/1.5 V=167 nA. Therefore, the intrinsic delay can be estimated to be: $\tau_{intrinsic}=C_pV_{DD}/I$=36 ns, corresponding to a maximum frequency of 4.5 MHz. For the as-fabricated device in this work, its operation speed is limited due to a large parasitic capacitance resulted from large overlapping area between the electrode pads and global gate. Superior frequency performance can be achieved by shortening the channel length, which in effect will reduce both gate capacitance and channel resistance, or by using a higher V_{DD}, which will reduce the carrier transit time in the channel.

11. A detailed comparison of BP inverter with reported 2D-related inverters.

Table S1. A detailed comparison of BP inverter in this work with reported 2D-related ones in terms of material use, supply voltage, logic-level match and complementary or not.

Ref	Channel material	Inverter Gain	Operation mode	Substrate	Gate dielectric	V_{DD} (V)	Logic match
This work	**Ex BP**	**5.7**	**CMOS**	**Si**	**50 nm Al_2O_3**	**0.3, 0.5, 1, 1.5**	**yes**
[1]	Ex ML MoS_2	4	NFET	Si/SiO_2	30 nm HfO_2	2	no
[2]	Ex BL MoS_2	5	NFET	Si/SiO_2	20 nm HfO_2	2	yes
[3]	Ex FL MoS_2	>30	NFET	Si/SiO_2 quartz	Al_2O_3	5	no
[4]	Ex BL WSe_2	25	CMOS	Si/SiO_2	60 nm Al_2O_3	5	no
[5]	Ex FL $MoTe_2$	1.3	CMOS	Si/SiO_2	SiO_2	10-20	no
[6]	Ex FL WSe_2	12	CMOS	Si/SiO_2	ZrO_2	1, 2, 3	yes
[7]	CVD graphene/MoS_2	12	NFET	Si/SiO_2	20 nm Al_2O_3	3	no
[8]	Ex n-MoS_2, Ex p-WSe_2	27	CMOS	Si/SiO_2 and glass	50 nm Al_2O_3	5	no
[9]	Ex BP	0.5	PFET Load R	glass	30 nm Al_2O_3	-1	no
[10]	Ex ML and FL ReS_2	4.4	NFET	Si/SiO_2	SiO_2	1, 2, 3	no
[11]*	Ex ML WSe_2	38	CMOS	Si/SiO_2	20 nm Al_2O_3	2-6	yes
[12]	n-MoS_2, p-WSe_2	2	Vertical CMOS	Si/SiO_2	Ion-Gel-Gate	0.5	yes
[13]	n-type CVD MoS_2, p-Si	16	hetero-CMOS	Flexible	50 nm Al_2O_3	1-5	yes
[14]	CVD graphene/MoS_2	6	NFET	Si/SiO_2	35 nm Al_2O_3	3-6	yes
[15]	10 nm MoS_2	1.5	CMOS	Si/SiO_2	50 nm SiO_2	0.5, 1, 2	no
[16]	n-type MoS_2, p-type BP	3.5	CMOS	Si/SiO_2	20 nm HfO_2	0.25-2.5	yes
[17]	CVD graphene and MoS_2	70	NFET	Si/SiO_2	ZrO_2	1, 2, 4	no
[18]	CVD ReS_2	3.5	NFET	Si/SiO_2	Ion-Gel-Gate	1	yes
[19]	Ex FL BP	5	CMOS	Si/SiO_2	SiO_2, hBN	5	no
[20]	Ex FL BP	~1	CMOS	Flexible	hBN	1, 2, 3	yes and no
[21]	CVD BL MoS_2	60	NFET	Si/SiO_2	22 nm Al_2O_3	5	yes
[22]	Ex BP	9.8	CMOS	Si/SiO_2	SiO_2	2, 3, 4	yes
[23]	Ex BP	46	CMOS	Si/SiO_2	30 nm hBN	2	yes
[24]	Ex BP	0.7	CMOS	Si/SiO_2	SiO_2	5	no
[25]	Ex $MoTe_2$	25	CMOS	Si/SiO_2	70 nm Al_2O_3	2, 4, 6	no
[26]	n-MoS_2, p-α-$MoTe_2$	33	CMOS	Glass	Al_2O_3	1, 3, 5	yes
[27]	Ex BP and MoS_2	150	CMOS	Si	HfSiO	1, 3	yes

EX – exfoliated; ML – monolayer; BL – bilayer; FL – few layer.

*Although not measured, the WSe_2-based CMOS inverter in [11] is likely to show a decent performance at V_{DD} =1 V.

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