Supplementary Information

In-memory Direct Processing based on Nanoscale Perpendicular Magnetic Tunnel Junctions

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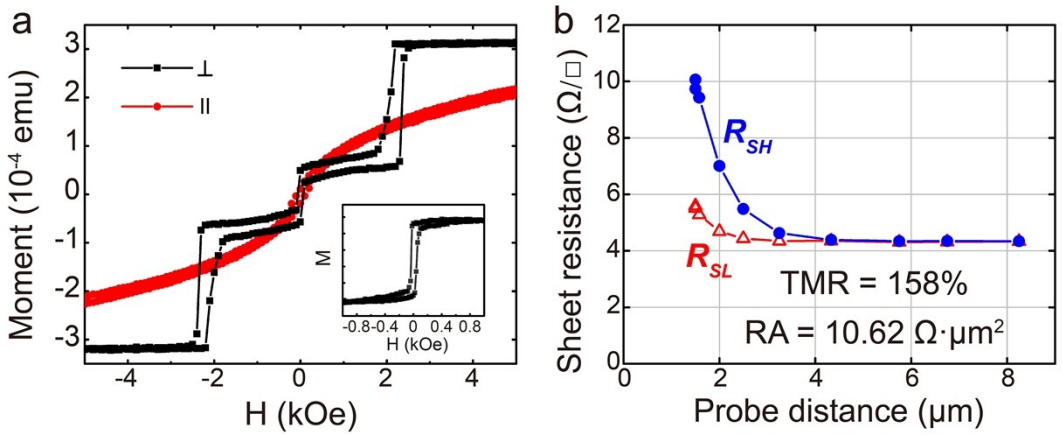
Supplementary Note 1. Film properties

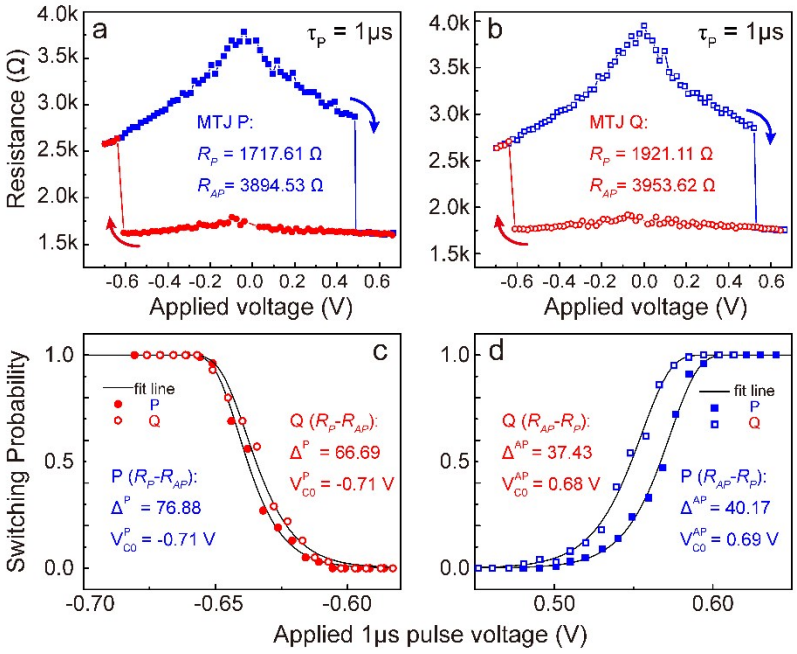


Supplementary Figure 1 | Film magnetic and magnetoresistance properties. a, Out-of-plane (⊥) and in-plane (||) magnetic fields induced hysteresis loops of the p-MTJ film annealed at 400℃ for 1 hour measured by VSM; inset is the minor loop. **b**, measured (symbol) and fitted (line) R_{SL} and R_{SH} of the p-MTJ film as a function of the probe distance, where the high sheet resistance state (R_{SH}) and low sheet resistance state (R_{SL}) are measured at the applied field of ±350Oe using CIPT tool.

Supplementary Figure 1a illustrates the representative M-H hysteresis loops under out-of-plane and in-plane magnetic fields, where the p-MTJ film annealed at 400℃ for 1 hour. The upper and bottom CoFeB free layers present strong ferromagnetic coupling and switch simultaneously according to the minor loop (inset of Fig. S1a), which is significant to enable STT switching. The strong coupling ensures the stability of the reference layer and synthetic antiferromagnetic (SAF) structure for high thermal stability and low stray field.

Supplementary Figure 1b shows the R_{SL} and R_{SH} of the p-MTJ film used to build devices as a function of the probe distance, where the R_{SH} and R_{SL} are measured at the applied field of ±350Oe, respectively. According to the fitting model[1] provided by Current In-Plane Tunneling (CIPT) method, the p-MTJ film has a TMR ratio of 158%, an RA of 10.62 Ω·μm^2, a sheet resistance of 44.58 Ω/□ for the top electrode, and a sheet resistance of the 4.79 Ω/□ for the bottom electrode.

Supplementary Note 2. Switching probability measurement using pulse voltage

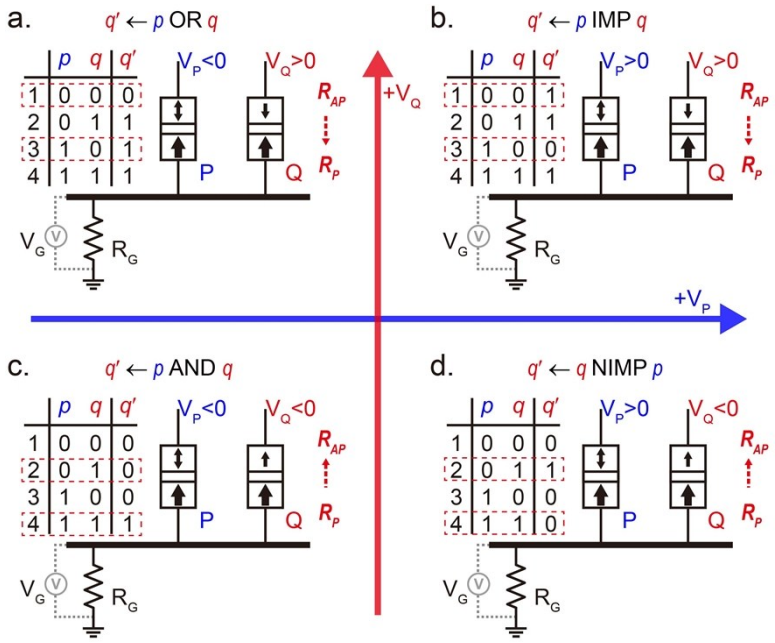


Supplementary Figure 2 | Electrical properties of p-MTJ devices used for building the basic logic circuit in this work. The STT switching loops are measured using voltage pulse with 1 μs duration of MTJ-P (**a**) and MTJ-Q (**b**). **c**, the switching probability behaviors from parallel states (P) to anti-parallel states (AP) of MTJ-P (red solid circles) and MTJ-Q (red hollow circles); **d**, the switching probability behaviors from AP to P of MTJ-P (blue solid squares) and MTJ-Q (red hollow squares), $\Delta^{P(AP)}$ and $V_{C0}^{P(AP)}$ were extracted from the fitting parameters, respectively.

Supplementary Figure 2a and 2b show the experimental STT switching behavior of the p-MTJ devices (P and Q used for building the basic logic circuit in this work) at room temperature (300*K*) and its detection by resistance change along with pulse voltage sweep with 1μs duration. The TMR is about 105% under -100mV pulse bias across the top electrodes.

In order to obtain critical voltage (V_{C0}) / (intrinsic spin transfer switching voltage at 0K) and thermal stability (Δ), the particular switching probability curves are presented in Fig. S2c and S2d, the whole measuring process is as follows (take the switching from AP to P as an example). The MTJ was first reset to AP state by applying a large minus voltage pulse (-0.75*V*). Then the large reset voltage was removed and the junction resistance was measured by applying a small readout voltage (-100*mV*) to ensure it in AP state. Subsequently, a short voltage switching pulse was applied to the junction. Finally, the junction resistance was measured by applying the readout voltage to determine whether it has switched or not. This sequence was repeated for 100 times to calculate the final switching probability under each condition. Each parameter extracted from the fitting is summarized as an inset, where the Δ is the average value of Δ^P and Δ^{AP}.[1-5]

Supplementary Note 3. Schematic of p-MTJs-based logic gate operation.



Supplementary Figure 3 | Schematic of p-MTJ-based logic gate operation. V_G is the voltage between common bottom electrode and GND. **a**, **b**, **c** and **d**, the truth tables, critical logic states and logic sequential voltage for the operation "OR", "IMP", "AND" and "NIMP", respectively.

A circuit analysis considering the basic logic processing circuit is carried out. Considering that the p-MTJ devices of the circuit shown in Fig. S3 behave as two resistances (R_P and R_Q) and applying Kirchhoff's current law at the R_G node, the voltage at node G is obtained as follows,

$$V_G = \frac{V_P R_G R_Q + V_Q R_G R_P}{R_P R_Q + R_G R_P + R_G R_Q} \quad (1)$$

V_G takes different values depending on the particular logic states, as different initial states (p and q) imply different values of R_P and R_Q. We will consider the effective applied voltage values between each p-MTJ device, V_P-V_G for P and V_Q-V_G for Q, respectively. In the logic states of the "IMP" logic truth table (as shown in Fig. S3b), the state of Q is changed only in case 1 (P and Q both in R_{AP}). V_Q-V_G must be positive because Q should be switched by STT from R_{AP} to R_P, which must remain at the Q initial state in the meantime when P is changed to R_P.

Considering that MTJ has a relatively symmetrical switching characteristic (R_{AP} to R_P and R_P to R_{AP}), we could obtain a truth table and logic operation similar to "IMP" (as shown in Fig. S3d), where the state of Q is changed only in case 4 (P and Q both in R_P). The logic of q NIMP p is achieved and its two simultaneous voltages are $V_P > 0$ and $V_G < 0$ after calculating the error ratio.

Similarly, "OR", "AND" logic operations can be performed when two processing voltages are $V_P < 0$, $V_G > 0$ and $V_P < 0$, $V_G < 0$, respectively (as shown in Fig. S3a and S3b).

Supplementary Note 4. The stable evaluations based on error rate distributions.

In order to figure out a suitable V_P and V_G, we used the calculation model and switching probability (as shown in equation (1)) of our p-MTJ devices to demonstrate the validity of the different logic. According to the logic truth table (as shown in Fig. S3), we defined the error of four different logic operations as:

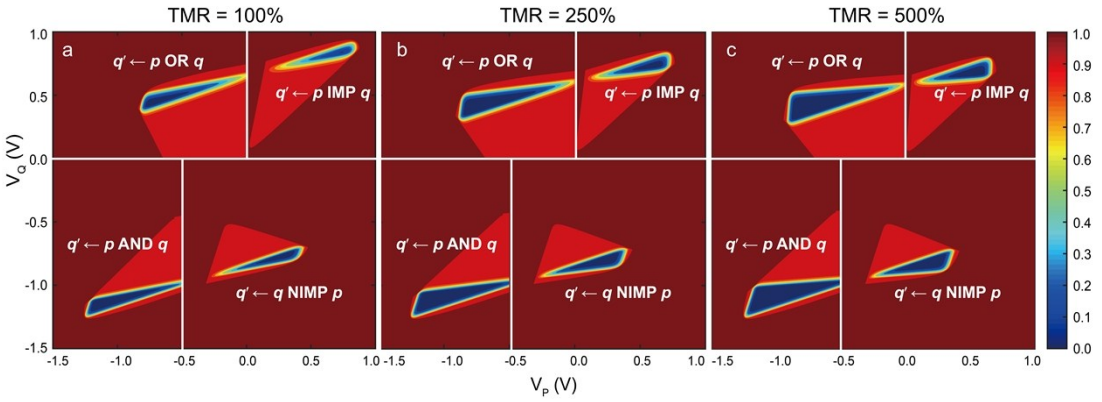
$$E_{IMP} = \left(1 - P_{Q1}^{AP}\right) + P_{P1}^{AP} + P_{Q3}^{AP} \quad (2)$$

$$E_{OR} = P_{Q1}^{AP} + \left(1 - P_{Q3}^{AP}\right) + P_{P3}^{P} \quad (3)$$

$$E_{AND} = \left(1 - P_{Q2}^{P}\right) + P_{Q4}^{P} + P_{P4}^{P} \quad (4)$$

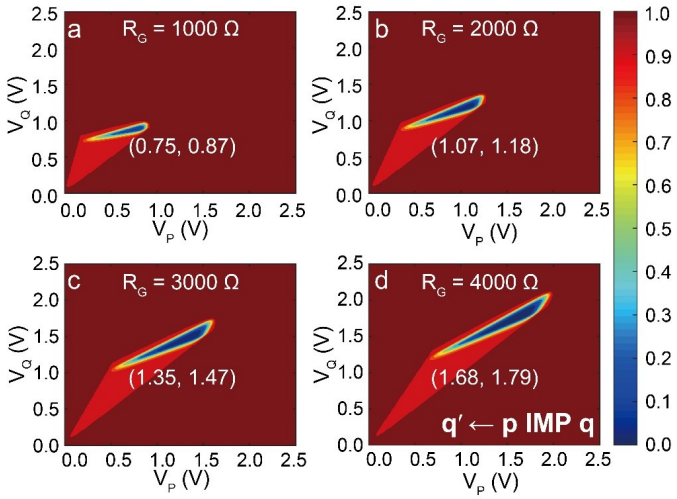
$$E_{NIMP} = P_{Q2}^{P} + P_{P2}^{AP} + \left(1 - P_{Q4}^{P}\right) \quad (5)$$

Where P is the switching probability for different devices, cases and states. For instance, $P_{Q1}{}^{AP}$ are defined as MTJ-Q's switching probability in case 1 from the AP to P. The analytical error rate distributions of different logic operations in this work were conducted under the model mentioned above. The used parameters were as follows: R_P = 1713Ω / 3619Ω (R_P / R_{AP} respectively), TMR_P ~ 110%, $V_{C0}{}^P$ = -0.71V / 0.69V and Δ_P = 77 / 40 (R_P - R_{AP} / R_{AP} - R_P respectively), R_Q = 1867Ω / 3953Ω, TMR_Q ~ 110%, $V_{C0}{}^Q$ = -0.71V / 0.68V and Δ_Q = 67 / 37 and R_G = 870Ω. All the resistance values were measured under -50mV dc bias and V_{C0} and Δ were obtained by fitting the switching probability curves (as shown in Fig. S2).



Supplementary Figure 4 | Stable evaluations based on error rate distributions. a, **b** and **c**, the error rate distributions of four different logic operations with TMR equal to 100%, 250% and 500% respectively.

Supplementary Figure 4 reals that the stability of "OR", "IMP", "AND", and "NIMP" gates will enhance with the increasing TMR value, when keeping all the parameters unchanged except for TMR (the resistance of R_{AP}). In general, TMR ~ 100% and R_G = 870 Ω were sufficient for robust behaviours of "OR", "AND", and "NIMP" gates.



Supplementary Figure 5 | IMP error as a function of V_P and V_Q. a, **b c** and **d**, the error rate distribution of IMP logic operation with RG equal to 1000Ω, 2000Ω, 3000Ω and 4000Ω respectively.

Supplementary Figure 5 demonstrates that the value of the IMP gate circuit parameters (such as RG) can be optimized to decrease the error for fixed pulse duration and the TMR. Our results show that increasing R_G within a certain range can significantly increase the stability window. However, the most appropriate process voltage values increase rapidly.

Supplementary References

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