Electronic Supplementary Information

Sub-kT/q Switching in In_2O_3 Nanowire Negative Capacitance Field-Effect Transistor

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1. Fabrication of the dual-gated transistor with NW suspending.

Fig. S1 Schematic illustrations of the fabrication process of the side-gated In_2O_3 NC-FETs: (a) A layer of MMA is spin-coated onto the Si/SiO₂ substrate followed by transferring In_2O_3 NWs; (b) Standard e-beam lithography is applied to define the source, drain and side-gate electrodes; (c) An HfO₂ buffer layer is deposited by ALD; (d) Ferroelectric P(VDF-TrFE) is assembled by spin-coating process at 2000 rpm, and then is baked on the hot plate at 130 °C for 30 min. (e) Fabrication processes in the cross-section view. (f) SEM image of the overall perspective of a double-gate device, the scale bar is 30 nm. The paired gate electrodes are connected by a metal wire. Inset is the SEM image of the device channel; the scale bar is 1 nm. The paired gate electrodes are connected by a metal wire.

2. Characterization of In₂O₃ NWs.



Fig. S2 (a) SEM image of the CVD growth In_2O_3 NWs, the scale bar is 1 µm. As shown in the image, the grown nanowires are uniform in thickness and the diameter of the nanowires is ~60 nm. (b) Transfer curves of a backgated In_2O_3 NW device fabricated on 100 nm SiO₂/Si substrate. (c) Output characteristics of the device.

3. Capacitance variation and electric field distribution for different channel architecture; ferroelectric hysteresis of the P(VDF-TrFE) film capacitor.



Fig. S3 (a) The capacitance versus the NW-to-gate distance for devices with single and double gate architecture. (b) Electric potential distribution in the cross-section of different architecture. (c) Electric field distribution in the cross-section of different architecture. (d) Electric field modulus distribution around the NW, and the x-axis is defined as the inset shows. The blue line, red line and yellow line represent the double gated with NW suspended architecture, the double gated without NW suspended architecture, respectively. (e) The ferroelectric hysteresis the P(VDF-TrFE) film capacitor. It is measured using Sawyer-Tower circuit at 1 Hz applied voltage frequency.

The capacitance is given by:

$$C = \frac{2\pi\varepsilon_0 \varepsilon_r L_{ch}}{\ln(4h/d)} \tag{1}$$

 ε_0 is the permittivity of free space, ε_r is the dielectric constant of PVDF, L_{ch} is the channel length, h is the thickness of the SiO₂ layer, and d (60 nm) is the NW diameter.

The electric field distribution in the channel region is simulated using a finite element analysis method. The parameters of the device architectures are designed as fellows: the diameter of the NW is 60 nm and the NW is

suspended 30 nm from the substrate; the thickness of the HfO_2 is 10 nm; the distance between two gate electrodes is 500 nm; the drain bias is 1V and the gate bias is 10 V.





Fig. S4 (a) Transfer curves of the In2O3 NW top-gated MOSFET. Transfer curves of In_2O_3 NW side-gated devices with different dielectric layer stacks: (b) device with the non-ferroelectric PMMA layer; (c) device with the ferroelectric PVDF layer. The inset of each figure shows the cross-section view structure of the corresponding device. The symbol "G" represents the gate electrodes in the schematic diagrams.

In the In₂O₃ NW top-gated MOSFETs, only a 6 nm layer of HfO₂ is deposited as the gate dielectric layer, as shown in the inset of Fig. R2a. The devices exhibit a significant counterclockwise hysteresis (Fig. R2a), indicating that there exist many interface traps in the HfO₂/gate electrode interface. We have further fabricated devices of the same dimensions and structure as the side-gated In₂O₃ NW NC-FETs, but without the ferroelectric layer in gate dielectric stacks. A non-ferroelectric PMMA layer is spin-coated onto the side-gated substrate after the ALD process, as shown in the inset of Fig. R2b. Since PMMA has no ferroelectric properties and can act as a passivation layer on the In₂O₃/HfO₂ channel, the device exhibits a small hysteresis window (Fig. R2b). Due to the inexistence of ferroelectric layer in gate dielectric stacks, both of the MOS device and the device with PMMA dielectric layer exhibit transfer characteristics with *SS* >60 mV/dec. In contrast, although the organic P(VDF-TrFE) layer can act as a passivation layer on the HfO₂ surface, a certain amount of hysteresis still appears in the NC-FETs (Fig. R2c), indicating that the hysteresis in the NC device is derived from the polarization of the ferroelectric. All of these indicate the negative capacitance effect of the ferroelectric P(VDF-TrFE) can efficiently lowering the *SS* values of the transistors below physic limit of 60 mV/dec.

Besides, there are also another two reasons for hysteresis in I_d - V_g curves of the NC-FETs. One is called as static hysteresis. Some papers have discussed this issue.^{1,2} The reason of static hysteresis is the mismatch of capacitances. To achieve the non-hysteretic I_d - V_g curves for In₂O₃ NW NC-FETs, the condition must be satisfied:

(1)

$$C_{\rm MOS} < C_{\rm FE} < C_{\rm OX}$$

where C_{mos} is a series combination of C_S and C_{OX} , and is defined as $C_{MOS}=C_SC_{OX}/(C_S+C_{OX})$. C_{OX} is the areal capacitance of HfO₂ oxide and C_S is the areal capacitance of In₂O₃ in our work. However, the C_S and C_{FE} are voltage dependent and size dependent. If the thickness of P(VDF-TrFE) (t_{FE}) is large, the capacitance mismatch ($C_{MOS} > | C_{FE} |$) will happen. As a result, there exists static hysteresis in I_d - V_g curves. Another kind of hysteresis is called as dynamic hysteresis. The reason is that there is a damping (resistive) term (ρ) in the dynamic Landau equation as shown in Eq. (2), which is not included in the static Landau equation.^{2,3} Unfortunately, almost all the published theoretical papers only take consideration of the static Landau equation.

$$V_{\rm gs} = V_{\rm MOS} + V_{\rm FE} = V_{\rm MOS} + 2t_{\rm FE}\alpha + 4t_{\rm FE}\beta Q^3 + 6t_{\rm FE}\gamma Q^5 + \rho t_{\rm FE}\frac{dQ}{dt}$$
(2)

where Q is the average gate charges density per area; α , β , and γ are Landau coefficients, which are material dependent constants; ρ represents the damping (resistive) term. However, the actual measurement process is dynamic because the rise time of the gate voltage cannot be infinite. So that internal gate voltage cannot follow the change speed of external gate voltage, which leads to the dynamic hysteresis. This kind of hysteresis cannot be eliminated in our work because copolymer P(VDF-TrFE) is comprised of long carbon chains, so its switching time (and ρ) becomes even larger due to huge mass and impediments by neighboring chains.⁴ So the hysteresis in this work is slightly changed and can't be eliminated.

5. Electrical performances of the side-gated In₂O₃ NW NC-FETs with different channel architecture.



Fig. 4 (a) The pinch-off voltage and hysteresis window as a function of t_{OX} . (b) Transfer curves of devices without the channel NW suspended. The HfO₂ thickness is 6 nm. (c) The SS versus V_{gs} data for devices without the channel NW suspended. The SS of the forward sweep does not present any value below 60 mV dec⁻¹, indicating that the suspended NW architecture brings larger gate coupling to the In₂O₃ NW NC-FETs. (d) Transfer curves with the gate leakage current of the side-gated NC-FETs. (e) Transfer curves with the gate leakage current of the self-aligned NC-FETs. (f) Gate leakage current density of the side-gated In₂O₃ NC-FET and the top-gated In₂O₃ MOSFET.

6. Low-temperature characteristics of transconductance (g_m) for different kinds of In_2O_3 NW FETs.



Fig. S5 (a) Transconductance versus V_{gs} at varying temperature for a side-gated In_2O_3 NW NC-FET. (b) Transconductance versus V_{gs} at varying temperature for a top-gated In_2O_3 NW MOSFET.

7. Schematic illustrations of the fabrication process and electric field interaction of the gate self-aligned In_2O_3 NC-FETs in cross-sectional views.



Fig. S6 (a) A suspended NW channel is fabricated without gate electrodes, and a 6 nm thick HfO_2 layer is deposited on the substrate. (b) An 8 nm Cr/Au film is over the channel region. (c) The gate leads are added onto the Cr/Au film and P(VDF-TrFE) film is spin-coated onto the entire substrate. (d) Electric potential distribution in the cross-section. (e) Electric field distribution in the cross-section. (f) The simulation results for electric field modulus distribution around the NW, and the x-axis is defined as the inset shows.

The electric field distribution in the channel region is simulated using a finite element analysis method. The parameters of the device architectures are designed as fellows: the diameter of the NW is 60 nm and the NW is suspended 30 nm from the substrate; the thickness of the HfO₂ is 6 nm and the thickness of the Au film is 8 nm; the drain bias is 0.1V and the gate bias is 2 V.

8. Hysteresis characteristics of the gate self-gated In₂O₃ NW NC-FETs.



Fig. S7 (a) Transfer characteristics of devices with L_{ch} values ranging from 100 nm to 3 μ m. (b) Transfer characteristics of the gate self-aligned In₂O₃ NW NC-FETs measured at room temperature, under V_{ds} of 0.1 V, 0.01V and 0.001 V. The channel length of the device is 200 nm and the V_{gs} sweep rate during measurement is 0.08 V s⁻¹.

9. Electrical performances of the self-aligned In_2O_3 NW NC-FETs without channel NW suspended.



Fig. S8 (a) Transfer characteristics of devices with L_{ch} values ranging from 100 nm to 1 μ m. (b) Detail plots SS as a function of L_{ch} . The performances of the gate self-aligned device without the channel NW suspended are quite worse than the suspended devices, because of the scarcity of ferroelectric between the gate tip and the NW channel.

10. Comparison of the In₂O₃ NW NC-FETs and the In₂O₃ NW MOSFETs.



Fig. S9 (a) Transfer characteristics of the gate self-aligned In_2O_3 NW NC-FET and the top-gated In_2O_3 NW MOSFET with $L_{ch}=1 \ \mu m$. (b) Transfer characteristics of the gate self-aligned In_2O_3 NW NC-FET and the top-gated In_2O_3 NW MOSFET with $L_{ch}=100 \ nm$. (c) Transfer characteristics of the back-gated In_2O_3 NW MOSFET with $L_{ch}=100 \ nm$.

The gate self-aligned NC-FETs exhibit superior modulation properties than the top-gated MOSFET structure and back-gated MOSFET structure, especially for short channel devices.

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