Electronic Supplementary Information

Mimicking biological neurons with a nanoscale ferroelectric transistor

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S1. FeFETs display a large I_{ON}/I_{OFF} ratio

When the transfer (I_D-V_G) curves are collected by using long integration time (e.g. >1 ms for each V_G point), the low current levels can be resolved in the picoampere range, revealing an I_{ON}/I_{OFF} ratio of more than 5 orders of magnitude, as shown in Figure S1.

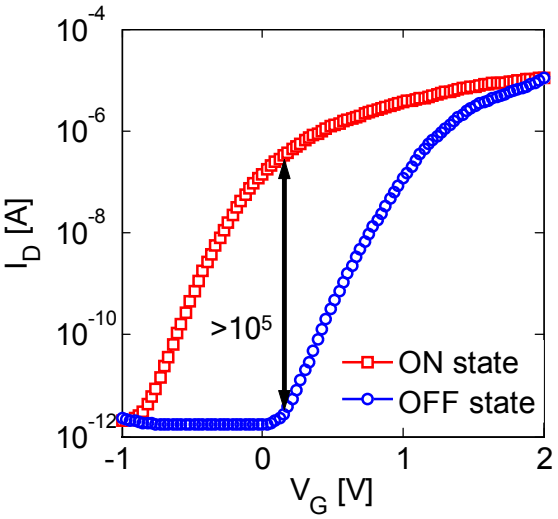

Figure S1 | Long-integration measurement of I_D-V_G curves for the two polarization states.

S2. Accumulative switching in large-area FeFETs

We have investigated the accumulative switching on large-area devices by considering a FeFET having $W = L = 1$ µm, made within the same process as the small-area devices considered in the main text. By applying a train of identical pulses having $V_P = 3$V and $t_P = 1$µs (Fig. 3a or inset Fig. S2), the switching appears to be very gradual Fig. S2 shows the evolution of threshold voltage and drain current as the number of pulses increases. It can be seen that the device displays a continuum of intermediate states, and the switching reaches the saturation after approximately 200 pulses.

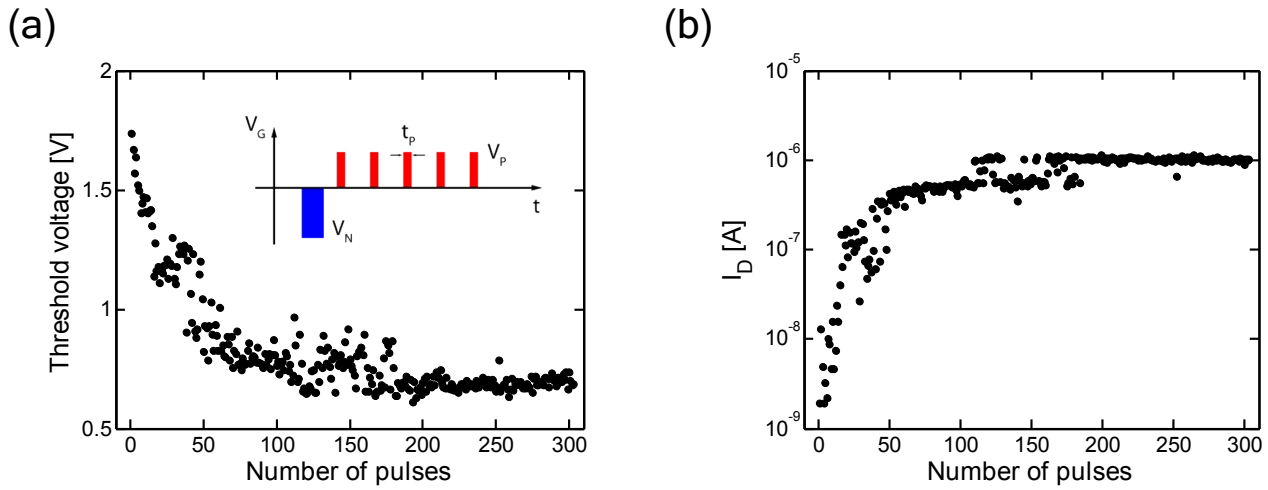

Figure S2 | Gradual accumulative switching in large-area FeFETs. (a) Threshold voltage and (b) drain current evolution upon a train of identical pulses ($V_P = 3$V, $t_P = 1$µs). Threshold voltage is extracted at $I_D = 0.1$µA $*W/L$.

S3. FDSOI FeFETs

The ultra-scaled devices having L=20nm and W=80 nm show a proper ferroelectric switching. Fig. S3 (a) shows the results of an experiment, in which the amplitude of a positive pulse was varied from 1 V to 4 V in order to induce the PRG transition. The switching occurs at around V_P= 2.5 V, t_P= 1µs.

The FDSOI FeFETs have an additional back-bias electrode. By changing its voltage V_{bb}, it is possible to tune the threshold voltage for both states of the transistor at desire, as shown in Fig. S3 (b).

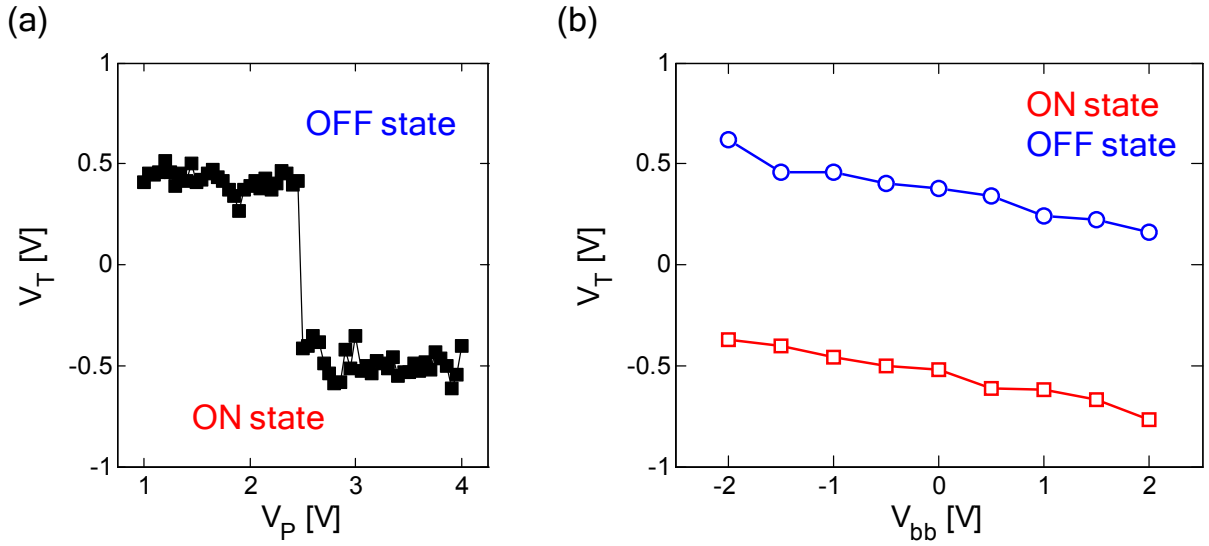

Figure S3 | Ferroelectric switching in FDSOI FeFETs. (a) Voltage dependent switching (b) Effect of the back-bias voltage V_{bb} on the threshold voltage for the two stored states.

S4. A possible circuital implementation of a FeFET based neuron

From the FeFETs physics it is clear that to program the device, positive voltage pulses exceeding the threshold voltage V_T have to be applied. In this way, a sufficient electric field is generated over the ferroelectric layer to induce polarization reversal. This, in turn, means that for each incoming positive pulse V_P of experiment in Fig. 3 (which are always larger than V_T), the FeFET will turn on, regardless whether it undergoes the PRG transition or not. From that perspective it becomes clear, that the evaluation of V_T of the FeFET can be performed by implementing a discrete time signal processing strategy in a clocked system, where programming and sensing is temporally separated.

An alternative solution is to use the current mode WTA circuit, originally proposed by Lazzaro et al. (1989),[1] as depicted in Fig. S4. This circuit can be used to compare the current flowing through the FeFET (transistor T1) with the current flowing through a reference transistor T2. Transistors T1 and T2 can be matched and the bias voltage V_{bn} can be set in a way that for the high-V_T state of the FeFET, transistor T2 always draws the larger current. Therefore the output voltage V_{out} will be always low, even for positive input pulse V_P at V_{in}. Only in case of the

polarization reversal of the FeFET (after PRG transition), which yields a lower threshold voltage for T1 compared to T2, the output voltage V_{out} will go high in response to a positive input pulse V_P at V_{in}. A feedback of V_{out} to the body of the FeFET could be used to erase the FeFET to its high- V_T state as soon as the input voltage pulse V_{in} ends, representing the reset operation discussed in section C).

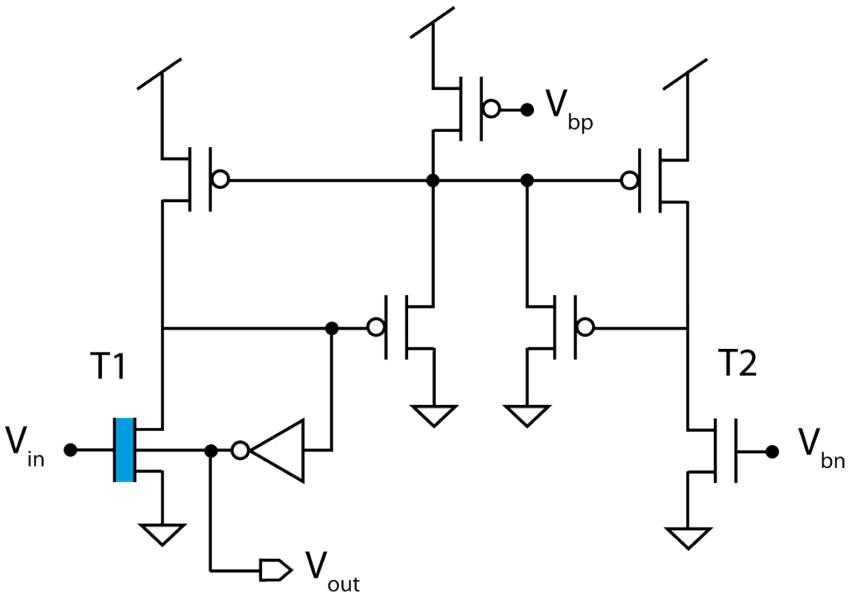

Fig. S4 A possible implementation a FeFET based neuron circuit. T1 is a FeFET, whereas T2 is a conventional transistor without a ferroelectric layer in the gate stack.

References

1 J. Lazzaro, S. Ryckebusch, M. A. Mahowald, C. A. Mead, Advances in neural information processing systems, 1989, **2**, 703-711.