Graphene-Si CMOS Oscillators

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Supporting Information

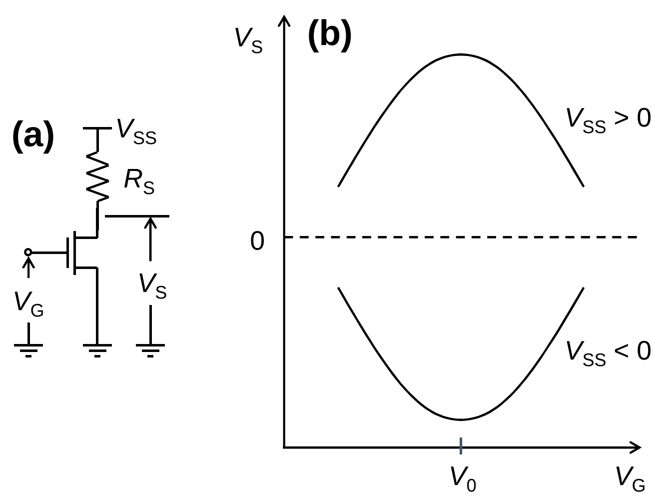

Figure S1: Static voltage transfer characteristic of the graphene circuit used in the oscillators. (a) The circuit comprises a graphene field-effect transistor (GFET) connected to a supply (V_{SS}) via load resistor (R_S). The resistance of the GFET (R_{ch}) depends on the applied gate voltage (V_G) and it reaches a maximum value $R_{ch,max}$ at the Dirac voltage ($V_G = V_0$). The output voltage of the circuit (V_S) is the voltage on R_{ch} and therefore $V_S = V_{SS}R_{ch}/(R_{ch} + R_S) = V_{SS}/(1 + R_S/R_{ch})$, corresponding to a simple voltage divider.[?] (b) The schematic of the static voltage transfer characteristic $V_S(V_G)$. The extreme value of this function is $V_S(V_0) = V_{SS}/(1 + R_S/R_{ch,max})$. The function has a maximum for $V_{SS} > 0$ and minimum for $V_{SS} < 0$.

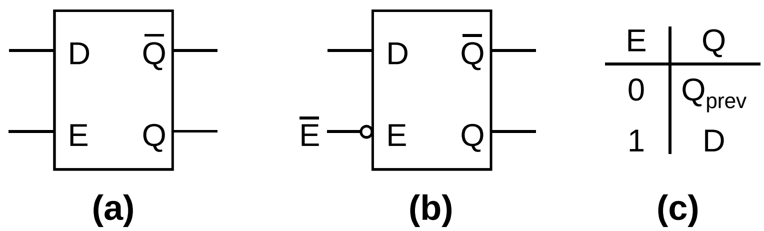

Figure S2: Gated D latch. (a) Schematic of a gated D latch which is enabled (active) when its enable line (E) is set high (1). This latch is used in the parabolic oscillator. (b) Schematic of a gated D latch which is enabled (active) when its enable line ($\overline{\mathrm{E}}$) is set low (0). This latch is used in the bow tie oscillator. (c) The truth table of a gated D latch. When the latch is enabled (E = 1), its output Q is equal to the data input D. Otherwise, the output Q stays in the previous state (Q_{prev}), i.e., the last state when the latch was enabled. If the oscillators are built from discrete components, the parabolic oscillator is simpler because most of the commercial D latches are type (a). This means that an additional inverter is needed to realize the D latch type (b), which is used in the bow tie oscillator.

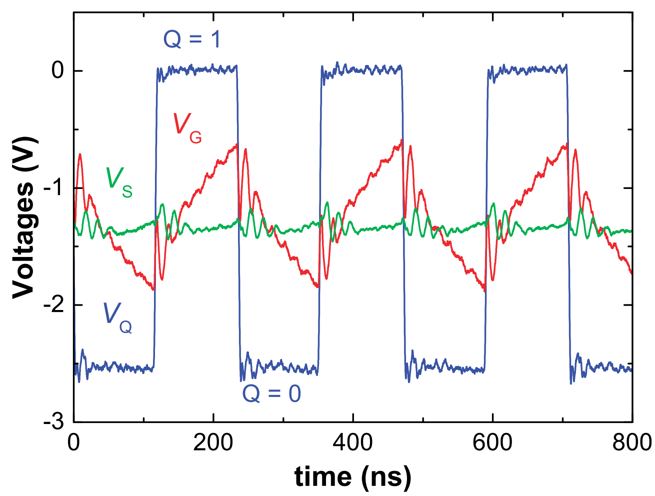

Figure S3: The waveforms measured in the parabolic oscillator exhibiting the highest oscillation frequency $f_{osc} = 4.2$ MHz which was possible to obtain with the used setup. The circuit parameters were $V_{SS} = -2.5$ V, $R = 300\ \Omega$, and $C = 0.5$ nF. The actual time constant of the RC timing circuit was slightly larger than RC due to additional capacitance of the cables used to connect the Si CMOS circuit to the GFET. A high-frequency (~ 60 MHz) disturbance visible in the waveforms is a consequence of multiple reflections in the cables used to connect the circuits.

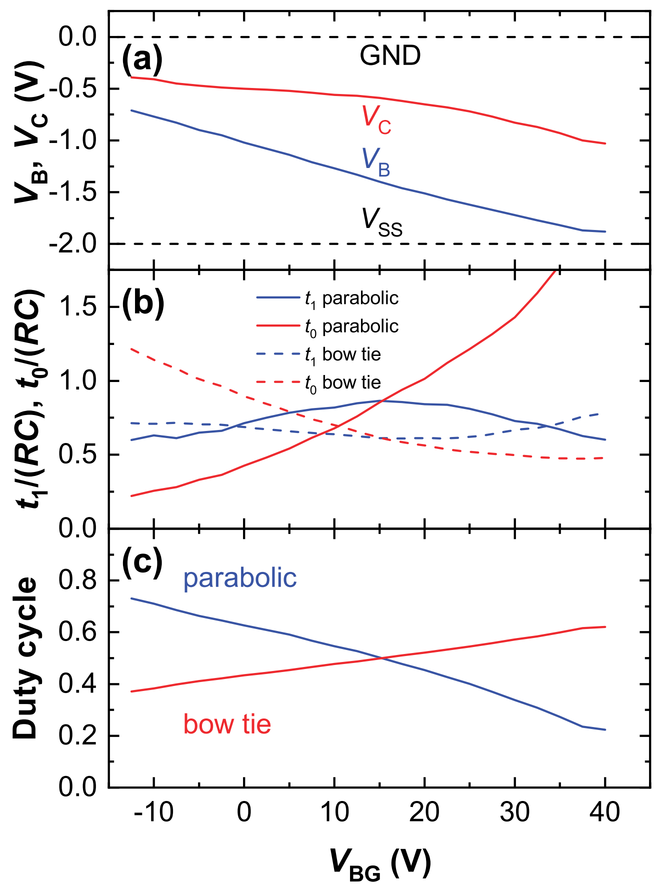

Figure S4: Calculated pulse width modulator (PWM) characteristics. (a) The intersection voltages V_B and V_C calculated from the measured static voltage transfer characteristics shown in Figure 3(a) in the main text. (b) Durations of the high (t_1) and low (t_0) state in the parabolic and bow tie oscillator calculated from the expressions for t_1 and t_0 in the main text and data in (a). (c) Duty cycle (D) in the parabolic and bow tie oscillator calculated as $D = t_1/(t_1 + t_0)$. In the parabolic oscillator, the calculated duty cycle ranges from 22 % to 73 %, which is very close to the duty cycle measured on the actual waveforms, as shown in Figure 3(b).

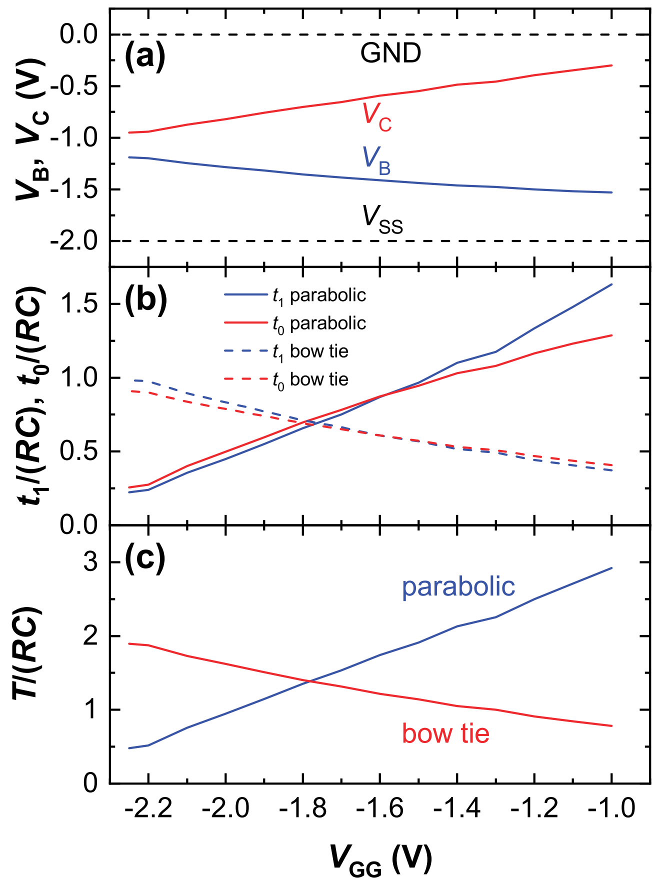

Figure S5: Calculated voltage-controlled oscillator (VCO) characteristics. (a) The intersection voltages V_B and V_C calculated from the measured static voltage transfer characteristics shown in Figure 4(a) in the main text. (b) Durations of the high (t_1) and low (t_0) state in the parabolic and bow tie oscillator calculated from the expressions for t_1 and t_0 in the main text and data in (a). (c) Period of oscillation (T) in the parabolic and bow tie oscillator calculated as $T = t_1 + t_0$. In the parabolic oscillator, the calculated period ranges from $0.48RC$ to $2.92RC$, corresponding to 28 kHz $< f_{osc} <$ 174 kHz, for R = 10 kΩ and C = 1.2 nF. This is very close to the oscillation frequency measured on the actual waveforms, as shown in Figure 4(b).