Electronic Supplementary Material (ESI) for Nanoscale.

Configurable multifunctional integrated circuits based on carbon nanotube dual-material gate devices

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Supporting information

S1. Threshold voltage calculation.

The method of calculating the threshold voltage (V_{th}) is shown in Figure S2.The V_{th} is calculated by the intercept of the line extrapolated at the point of maximum transconductance.

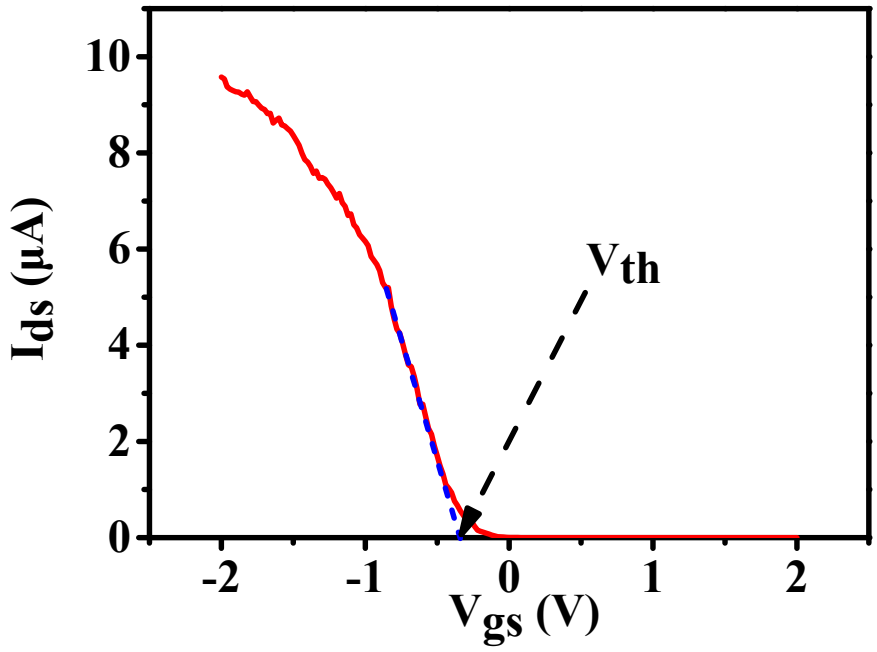

Figure S1. Method of V_{th} calculation.

S2. Transfer characteristics of a typical DMG and NG device in FET mode.

The transfer characteristics of the DMG device and NG device were measured under the drain-to-source bias (V_{ds}) from -0.2 V to -1 V. Both the DMG and NG device here were fabricated on the same CNT with fixed oxide thickness of 10nm.

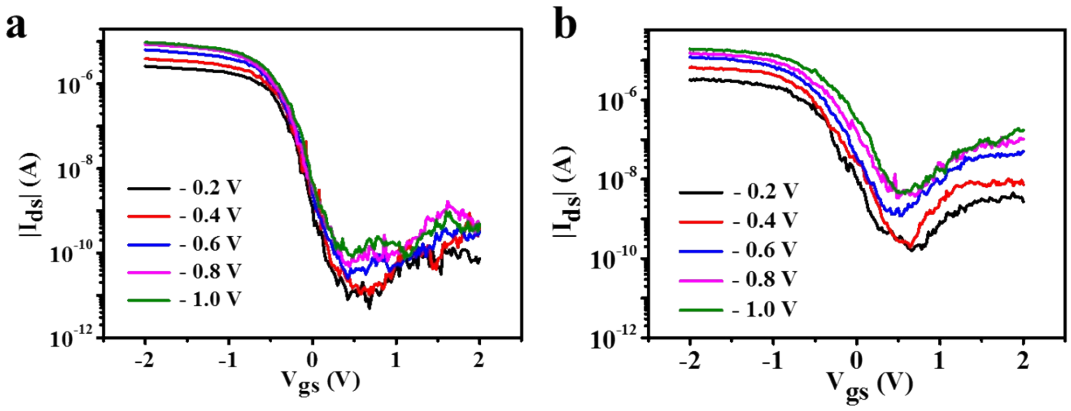

Figure S2. (a) Transfer characteristics of the DMG device in FET mode. (b) Transfer characteristics of the NG device in FET mode.

S3. I-V curves of a typical DMG device in diode mode.

The *I-V* curves of a DMG devices in diode mode was shown in Figure S3. Figure S3a demonstrated different rectifying behaviors whether the gate electrode was floated or not. The rectifying behavior under different gate-to-source voltage (V_{gs}) were present in Figure S3b.

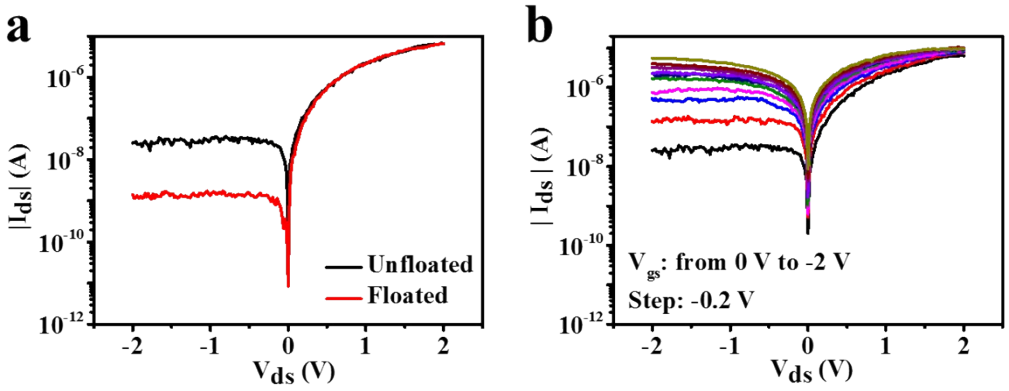

Figure S3. (a) The I-V curve of a typical DMG device whether the gate electrode is floated (red curve) or not (black curve) (b), The I-V curves of a DMG device under different V_{gs}.

S4. SEM images of the DMG devices with different metal length ratio.

The DMG devices were constructed on the same CNT with fixed total gate length of 500 nm and oxide thickness of 10 nm. The metal (closer to the drain) was evaporated with 20 nm Pd. The metal closer to the source was evaporated with 30 nm Y.

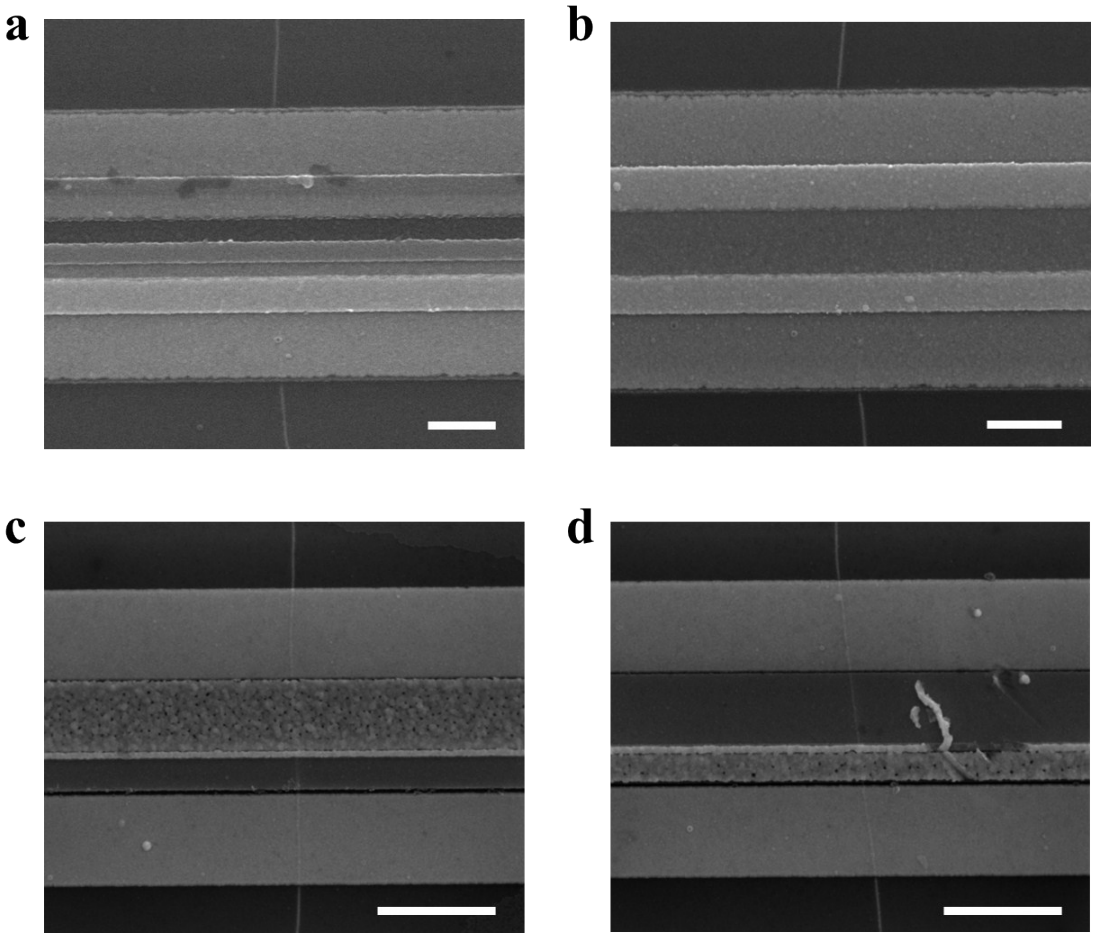

Figure S4. SEM images of the DMG devices with different length ratio. (a) L_{Pd} : L_Y= 1:1. (b) L_{Pd} : L_Y= 1:0. (c) L_{Pd} : L_Y= 1:3. (d) L_{Pd} : L_Y= 3:1.The scale bar represent 500 nm.

S5. Characteristics of the on-chip resistor

The on-chip resistors were designed by Ti wires with thickness of 4 nm, width of 4 μm and length of 1.5 mm. The detailed characteristics of a typical resistor is demonstrated in Figure S5.

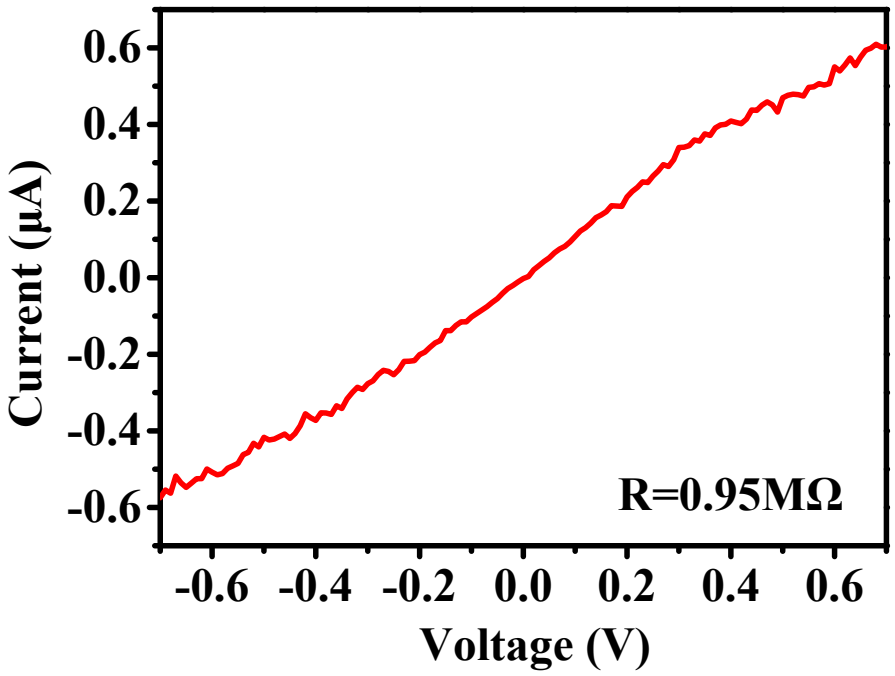

Figure S5. Resistance of the Ti wire.

S6. The equivalent circuits of the analog IC.

The DMG device, together with the on-chip resistor, form an analog IC. The configurations are detailed in Figure S6. Under the rectifier configuration, the input terminal V2 was floated, the AC signal was input from the V1 terminal. At this situation, the DMG device are equivalent to a diode paralleled with a very large resistor. Thus the whole circuits can be regarded as a rectifier. When operated as a source follower, V1 terminal was connected to the negative bias V_{dd} = -2 V, while the input AC signal together with a quiescent bias of -1 V was applied on V2 terminals. Under this configuration, the diode is negatively biased and can be regarded as a very large resistor. Thus whole circuits can be considered as a source follower.

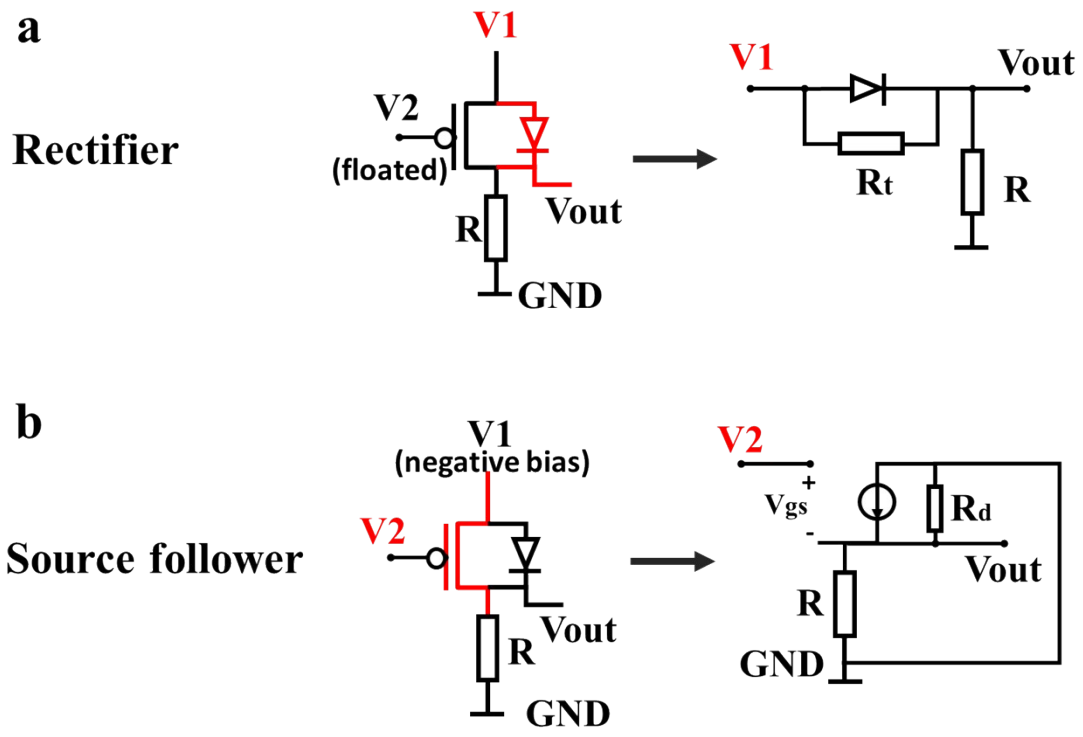

Figure S6. The equivalent circuit diagram of the analog IC. The red line represent the branch is selected in conduction state.

S7. The equivalent circuits of the digital IC.

The DMG devices can construct digital IC together with two on-chip-diode. The configuration is detailed in figure S7. When configured as a NOR gate, the V1 and V4 terminal are connected to the Vdd = 2 V and ground (GND).The digital signals were input from the V2 and V3 terminal. At this situation, the circuit can be regarded as two p-type transistors with a pull-down resistor, that is a NOR gate. Under the AND configuration, the V2 and V3 terminal are floated, while the digital signal V1 and V4 terminal. At this situation, the whole circuit can be equivalent to a AND gate using two diodes and a pull-up resistor.

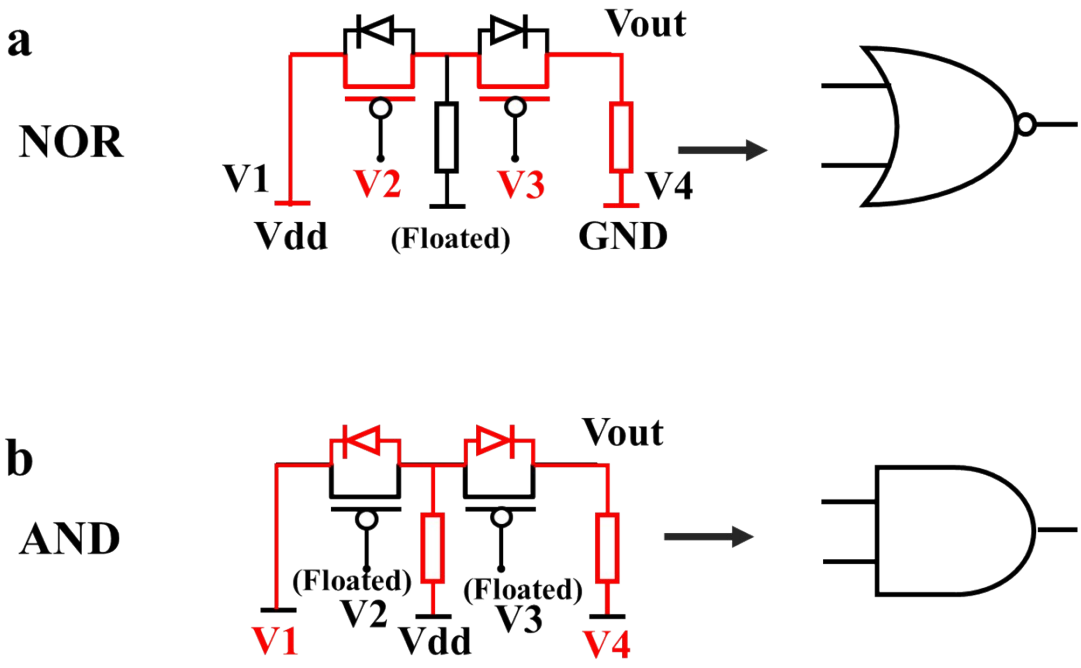

Figure S7. The equivalent circuit diagram of the digital IC. The red line represent the branch is selected in conduction state.