Electronic Supplementary Material (ESI) for Nanoscale.

Supplementary Materials

High-Performance Sub-10 nm Monolayer Bi_2O_2Se Transistors

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Table S1. Benchmark of the ballistic performance upper limits of the ML Bi_2O_2Se MOSFETs against the ITRS 2.0 2013 edition requirements for HP devices.

	L_g (nm)	**EOT (nm)**	**V_{dd} (V)**	**UL (nm)**	**I_{on} (μA/μm)**	**C_{total} (fF/μm)**	**τ (ps)**	**PDP (fJ/μm)**
n-type	1.0	0.41	0.64	0	–	0.06	–	0.025
				2	0.2	0.06	183	0.025
				4	130	0.03	0.261	0.012
p-type				0	0.6	0.09	117	0.037
				2	67	0.09	0.522	0.037
				4	296	0.06	0.099	0.025
n-type	2.0	0.41	0.64	0	–	0.15	–	0.061
				2	1.7	0.15	51	0.061
				4	871	0.09	0.072	0.037
p-type				0	2.3	0.15	42	0.061
				2	470	0.12	0.180	0.049
				4	569	0.15	0.165	0.061
n-type	3.0	0.41	0.64	0	–	0.21	–	0.086
				2	285	0.12	0.267	0.049
				3	996	0.15	0.093	0.061
p-type				0	52	0.18	2.334	0.074
				2	1127	0.27	0.102	0.111
n-type	5.0	0.41	0.64	0	306	0.36	0.762	0.147
				2	2067	0.30	0.093	0.123
p-type				0	1147	0.39	0.219	0.160
ITRS HP 2028	5.1				900	0.60	0.423	0.240
n-type	6.7	0.47	0.68	0	2126	0.39	0.126	0.180
p-type				0	1840	0.54	0.204	0.250
ITRS HP 2025					1100	0.77	0.451	0.360
n-type	8.8	0.54	0.72	0	3380	0.48	0.102	0.249
p-type				0	1819	0.72	0.285	0.373
ITRS HP 2022					1350	0.87	0.463	0.450

Table S2. Benchmark of the ballistic performance upper limits of the ML Bi_2O_2Se MOSFETs against the ITRS 2.0 2013 edition requirements for LP devices.

	L_g (nm)	**EOT (nm)**	**V_{dd} (V)**	**UL (nm)**	**I_{on} (μA/μm)**	**C_{total} (fF/μm)**	**τ (ps)**	**PDP (fJ/μm)**
n-type	1.0	0.41	0.64	0	–	0.12	–	0.049
				2	–	0.15	–	0.061
				4	–	0.15	–	0.061
p-type				0	–	0.06	–	0.025
				2	–	0.12	–	0.049
				4	0.4	0.09	144	0.037
n-type	2.0	0.41	0.64	0	–	3.00	–	1.229
				2	–	3.00	–	1.229
				4	–	0.30	–	0.123
p-type				0	–	0.21	–	0.086
				2	3.8×10^{-3}	0.21	3.5×10^{4}	0.086
				4	46.8	0.06	0.821	0.025
n-type	3.0	0.41	0.64	0	–	0.42	–	0.172
				2	–	0.45	–	0.184
p-type				0	6.1×10^{-4}	0.33	3.5×10^{5}	0.135
				2	1.7	0.09	34	0.037
n-type	5.0	0.41	0.64	0	–	0.63	–	0.258
				2	4.1×10^{-3}	0.63	9.8×10^{4}	0.258
p-type				0	0.2	0.39	1.2×10^{3}	0.160
				2	2.9	0.24	53	0.098
ITRS LP 2028	5.9				295	0.69	1.493	0.280
n-type	7.0	0.45	0.66	0	3.8×10^{-3}	0.78	1.4×10^{5}	0.340
p-type				0	411	0.42	0.674	0.183
ITRS LP 2026					337	0.77	1.514	0.340
n-type	9.3	0.51	0.71	0	10	0.81	57.5	0.408
p-type				0	830	0.45	0.385	0.227
ITRS LP 2023					458	0.95	1.474	0.480

Table S3. Benchmark of the ballistic performance upper limits of the ML MoS_2 MOSFETs against the ITRS 2.0 2013 edition requirements for HP devices.

	L_g (nm)	**UL (nm)**	**EOT (nm)**	**V_{dd} (V)**	**I_{on} (μA/μm)**	**C_{total} (fF/μm)**	**τ (ps)**	**PDP (fJ/μm)**
n-type	1	0	0.41	0.64	4	0.11	17.280	0.015
		2			61	0.11	1.102	0.015
		4			113	0.10	0.578	0.014
p-type		0			34	0.10	1.864	0.014
		2			293	0.09	0.190	0.012
		4			283	0.07	0.149	0.009
n-type	5	0	0.41	0.64	216	0.63	1.867	0.086
		2			230	0.56	1.544	0.076
p-type		0			519	0.45	0.555	0.061
		2			598	0.32	0.344	0.044
ITRS HP 2028	5.1			0.68	900	0.60	0.423	0.240
n-type	9	0	0.51	0.64	230	1.26	3.506	0.172
p-type					510	0.84	1.054	0.115
ITRS HP 2022	8.8			0.72	1350	0.87	0.463	0.450

Table S4. Simulation parameters of the sub-10 nm MOSFETs. All the devices are simulated at the DFT+NEGF level and double gate configurations. The source and drain are degenerately doped with the doping concentration ρ.

	channel material	basis set	V_{dd} (V)	ρ (cm^{-2})
n-type	Bi_2O_2Se	DZP	0.64 – 0.72	5×10^{13}
	MoS_2	DZP	0.64	5×10^{13}
	InSe	DZP	0.64	1×10^{13}
	Arsenene	DZP	0.64 – 0.72	$(1\text{–}5) \times 10^{13}$
	Antimonene	DZP	0.64	1×10^{13}
p-type	Bi_2O_2Se	DZP	0.64 – 0.72	5×10^{13}
	MoS_2	DZP	0.64	5×10^{13}
	InSe	DZP	0.64	9×10^{13}
	Phosphorene	SZP	0.69 – 0.78	4×10^{13}

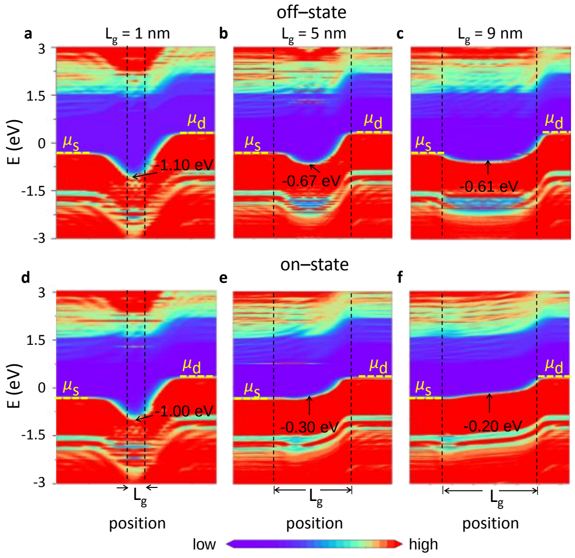

Fig. S1. Comparison of the local density of states of the ML Bi_2O_2Se *p*-MOSFETs at the off- and on-states with different gate length. UL = 0 nm. μ_s and μ_d are the electrochemical potential of the source and drain, respectively. The off-state has a current of 0.1 μA/μm, and the on-state is the state with a gate difference of V_{dd} = 0.64 V to the off-state. The energy of VBM at the middle of the channel (E_{mid}) is labeled.

The comparison of the local density of states of the ML Bi_2O_2Se *p*-MOSFETs with different gate lengths is shown in Fig. S1. To evaluate the modulation of the band edge location by gate voltage, the energy of the valence band edge at the middle of the channel (E_{mid}) is labeled. No UL is considered in this comparison. To achieve the current of 0.1 μA/μm at the off-state, E_{mid} at L_g = 1 nm is the lowest, followed by those at L_g = 5 nm and 9 nm. With a gate voltage variation of 0.64 V, the changes of E_{mid} at L_{g} = 1 nm, 5 nm and 9 nm are 0.10 eV, 0.37 eV and 0.41 eV, respectively. The enhanced modulation of E_{mid} suggests the improved gate controllability and this trend is consistent with smaller SS at longer L_{g}.

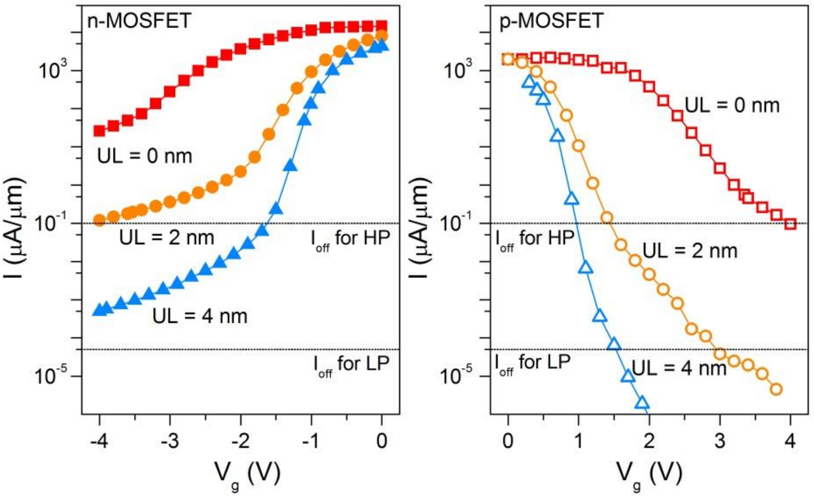

Fig. S2. Transfer characteristics of the ML Bi_2O_2Se MOSFETs with different underlaps. L_{g} = 1 nm. The supply voltage is set to 0.64 V.

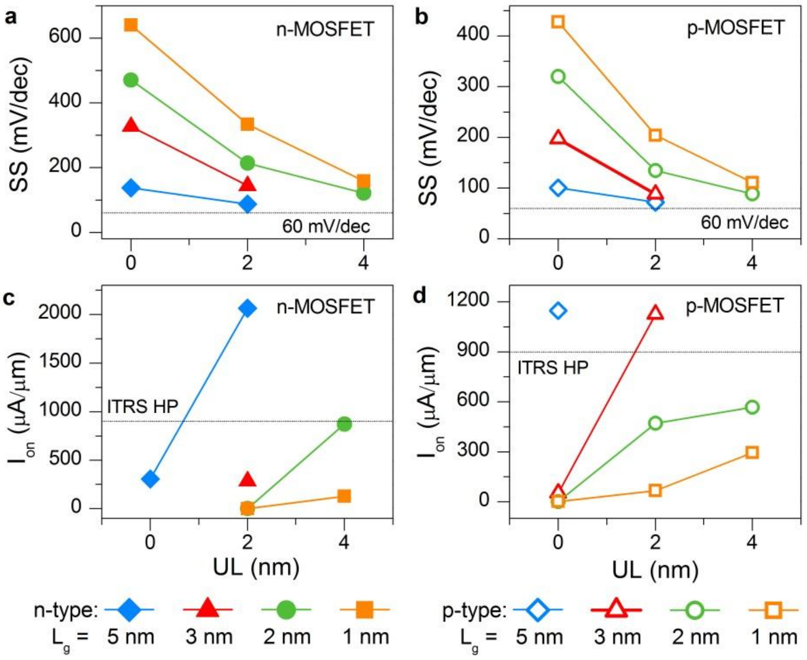

Fig. S3. SS and on-current of the ML Bi_2O_2Se MOSFETs as a function of UL. The supply voltage is set to 0.64 V.

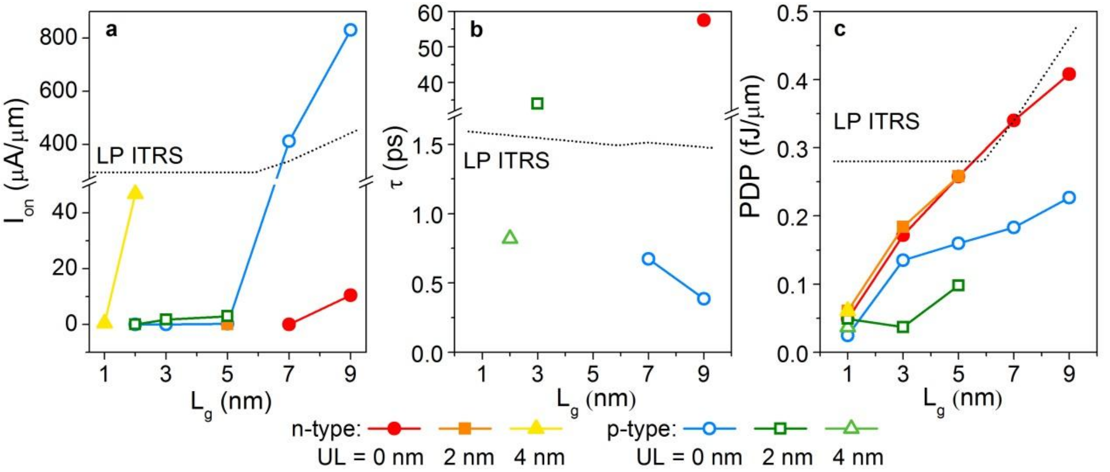

Fig. S4. On-current, delay time and power dissipation of the ML Bi_2O_2Se MOSFETs as a function of the gate length for LP applications. V_{dd} = 0.64 ~ 0.71 V.

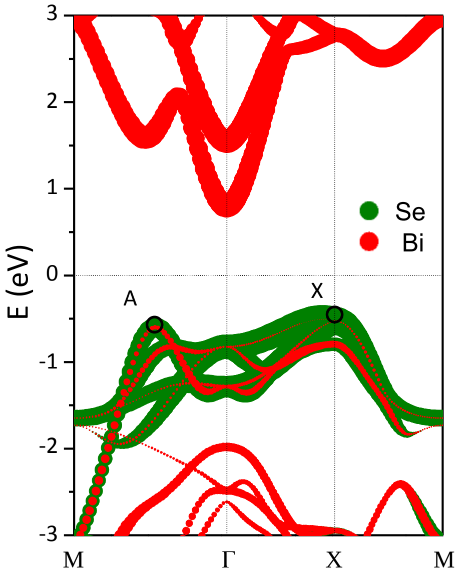

Fig. S5. Band structure of ML Bi_2O_2Se calculated by using the plane wave basis set and projector augmented wave (PAW) potential, as implemented in the VASP code. The green and red points stand for the contributions from Se and Bi atoms, respectively, and the size of the points is proportional to the contribution weight.

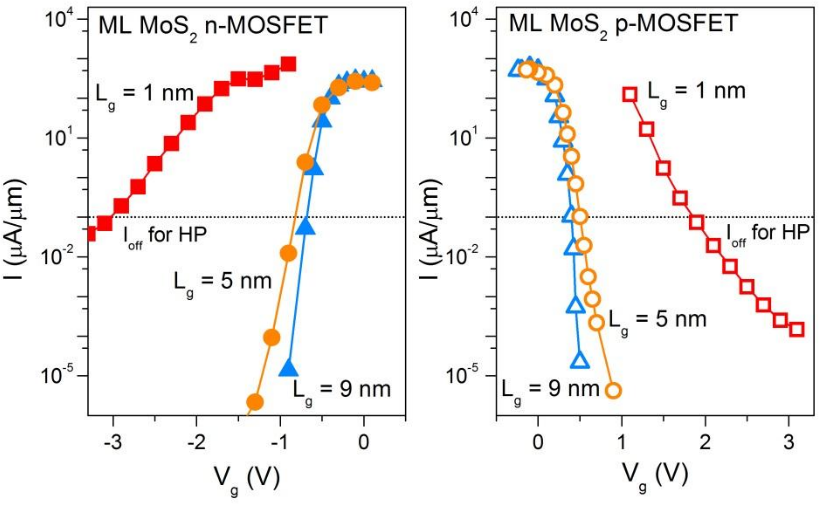

Fig. S6. Transfer characteristics of the ML MoS$_2$ MOSFETs with different gate length. UL = 0 nm. The supply voltage is set to 0.64 V.