Electronic Supplementary Material (ESI) for Nanoscale.

Supporting Information for

Negative transconductance and negative differential resistance in asymmetric narrow bandgap 2D-3D heterostructure

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Supplementary section 1:

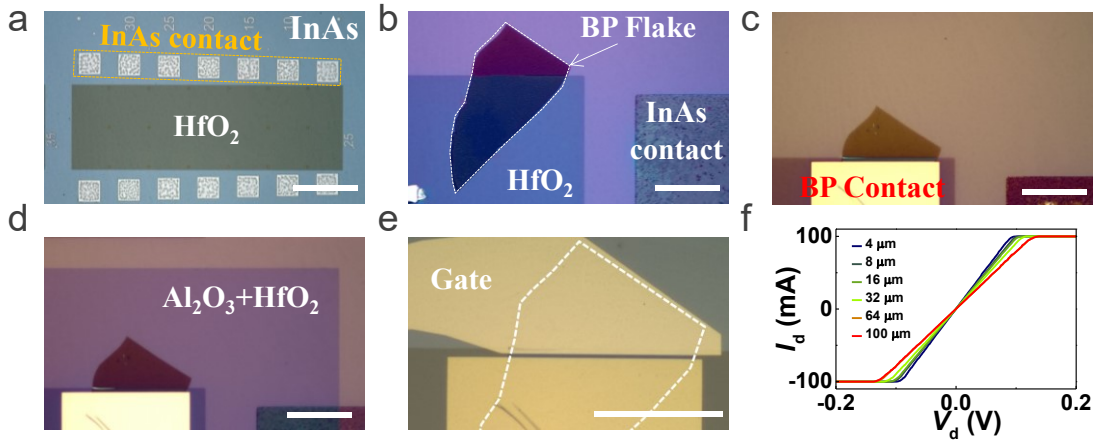


Figure S1 | Fabrication process of BP/InAs device. For fabricating the BP/InAs heterostructure, we start with InAs wafer and deposit 20 nm Ti/60 nm Au as the Ohmic contact to InAs. Then, 20 nm insulating dielectric HfO_2 was deposited at 250 °C by atomic layer deposition (ALD), followed by rapid thermal annealing (RTA) at 500 °C for 30 s in a nitrogen ambient to improve the dielectric film quality. Next, the HfO_2/InAs wafer was patterned using photolithography and the dielectric HfO_2 was selectively etched using inductively coupled plasma (ICP). (**a**) The engineered substrate comprises the InAs contacts and the insulating region. Scale bar, 200 μm. (**b**) The BP flake was exfoliated and transferred onto the substrate, part of the BP flake overlaps with the InAs while the other part stacks on the HfO_2. Scale bar, 20 μm. (**c**) A stack of 20 nm Ni/60 nm Au was deposited as BP contact. Scale bar, 20 μm. (**d**) The gate dielectric stack contains 5 nm Al_2O_3 by natural oxidation of Al and 10 nm HfO_2 by ALD. Scale bar, 20 μm. (**e**) A stack of 20 nm Ni/60 nm Au gate electrode was deposited to complete the device. Scale bar, 20 μm. There is no overlapping region between the BP contact and the gate electrode. (**f**) The two terminal I–V characteristics of the InAs devices at 300 K with various channel length, showing an excellent Ohmic contact.

Supplementary section 2:

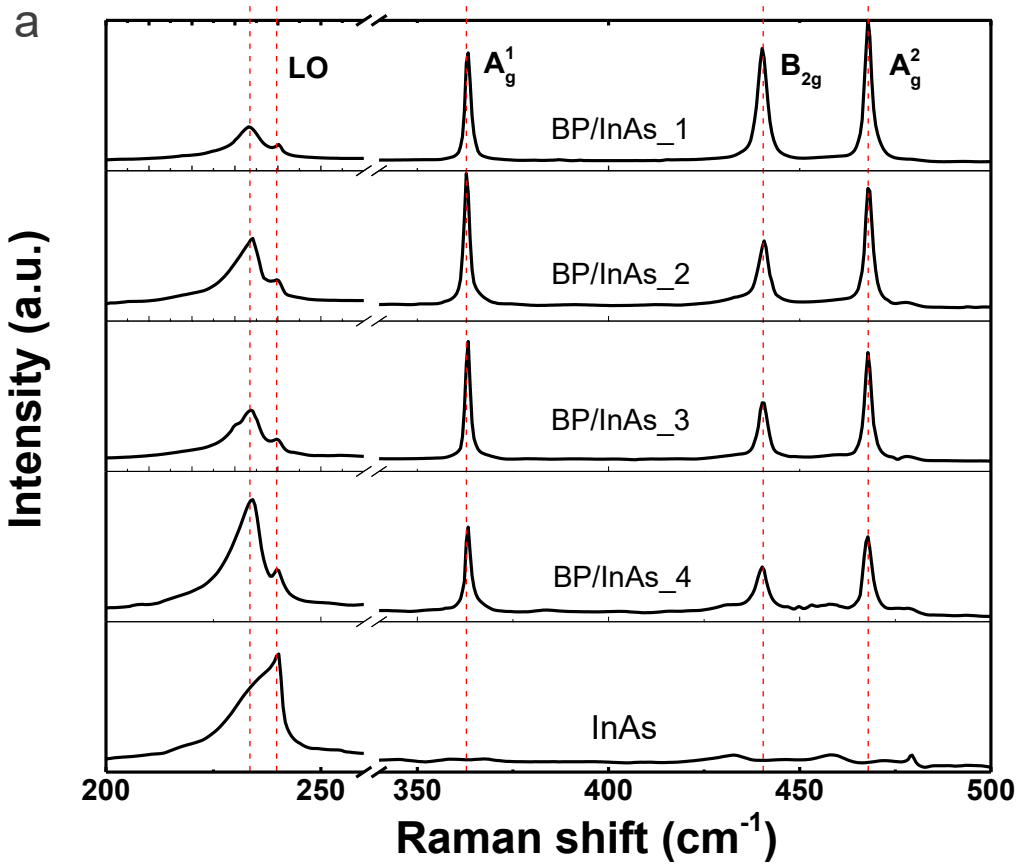
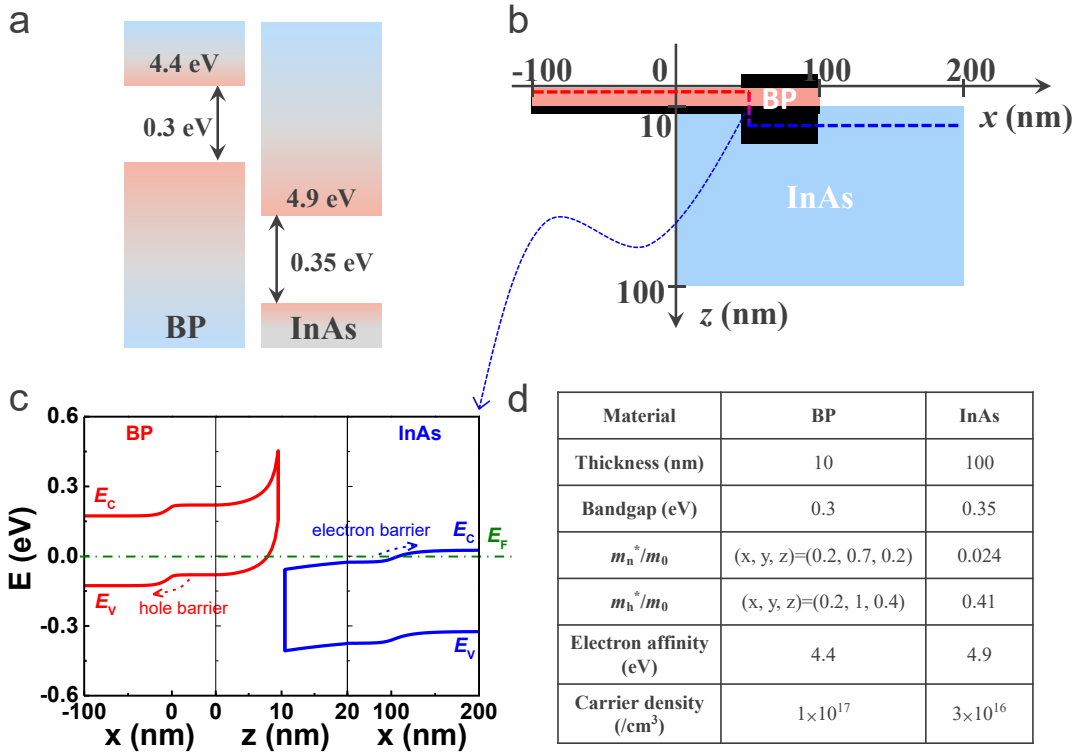


Figure S2 Raman spectra measured with a 532 nm excitation laser on different BP/InAs heterostructures on the same wafer.

Supplementary section 3:



Material	BP	InAs
Thickness (nm)	10	100
Bandgap (eV)	0.3	0.35
m_n^*/m_0	(x, y, z)=(0.2, 0.7, 0.2)	0.024
m_h^*/m_0	(x, y, z)=(0.2, 1, 0.4)	0.41
Electron affinity (eV)	4.4	4.9
Carrier density (/cm^3)	1×10^{17}	3×10^{16}

Figure S3 | Simulation details. To determine the band alignment at the BP/InAs heterointerface, we calculate the 2D band diagram in the parallel and vertical directions of the BP/InAs heterostructure using nextnano software. These simulations do not consider BTBT or other transport mechanisms, and also do not consider the interaction between electronic orbital positions of the different layers but the carrier density, bandgaps, and band alignment. (**a**) Energy-band diagrams for isolated BP and InAs with different bandgap and electron affinity. The energy band alignment is type-III broken-gap, which meets the band alignment requirement for interband tunneling. (**b**) Schematic view of the BP/InAs heterostructure that is used for simulation of the band diagrams. The thickness of BP flake and InAs are 10 nm and 100 nm, respectively. The length of the access region and BP/InAs overlapping region all are 100 nm. (**c**) The band alignment of the heterostructure along the blue dashed line in Figure S3b. A horizontal hole potential barrier is naturally formed at the boundary due to the

inhomogeneous carrier distribution in the access BP region and the BP/InAs overlapping region. The barrier at the InAs side is very small and can be ignored. (**d**) The detailed materials parameters used in the simulations for BP/InAs heterostructures.

Supplementary section 4:

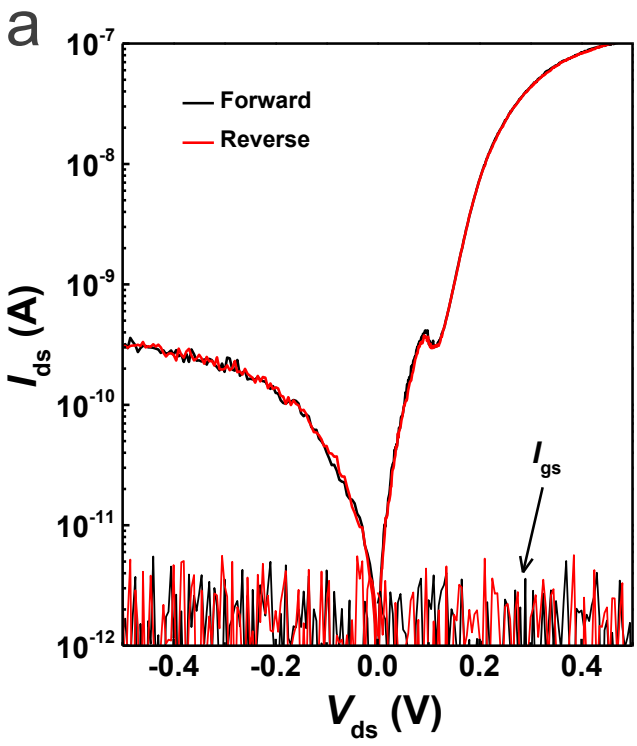


Figure S4 (**a**) The double-sweep output characteristics of the BP/InAs device, showing an NDR behavior for both forward and reverse sweeps. And the gate leakage current is small enough compared with drain current.

Supplementary section 5:

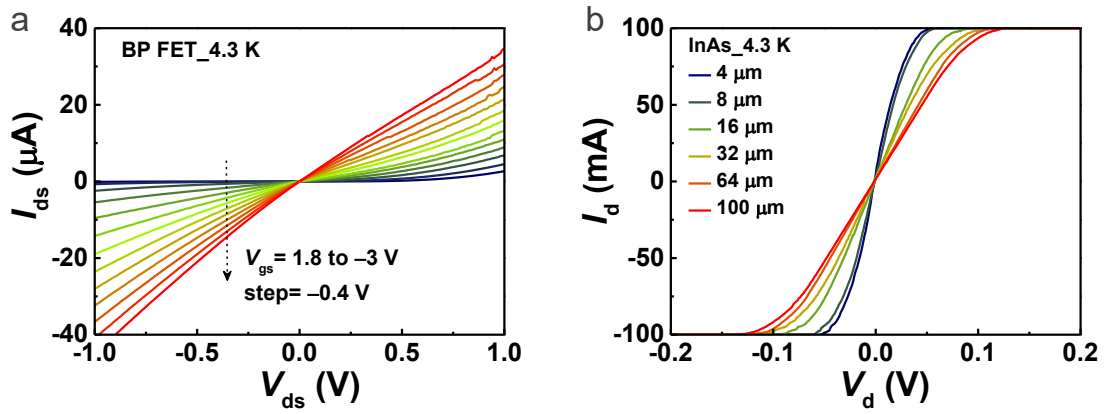


Figure S5 (**a**) The I_{ds}–V_{ds} curves of the BP FET at 4.3 K, with V_{gs} changing from 1.8 V to –3 V with a step of –0.4 V. (**b**) The two terminal I–V characteristics of the InAs devices at 4.3 K with various channel length. The metal contacts on BP and InAs show a good ohmic at 4.3 K.