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#### **Supplementary Information**

# Dynamics of bias instability in the tungsten-indium-zinc oxide thin film transistor

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**S1.** Schematic of the overall bottom-gate structured WIZO TFT fabrication. (a)  $SiO_2/p^{++}-Si$  substrate, (b) WIZO deposition with a pattern by RF sputtering with various active layer thickness, (c) patterned ITO as a source/drain electrode, (d) post-annealing process using furnace system at 250 °C in ambient air for 1 h, and (e) bottom-gate structure WIZO TFT with channel width and length of 800 and 200  $\mu$ m, respectively.

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**S2.** Comparison of the device performance of the WIZO-TFT and IGZO-TFT fabricated with each optimization condition, and the same post-annealed at 250 °C for 1 hour.

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**S3.** The change of device parameter as a function of bias stress time