Electronic Supplementary Material (ESI) for Journal of Materials Chemistry C.

Supporting Information

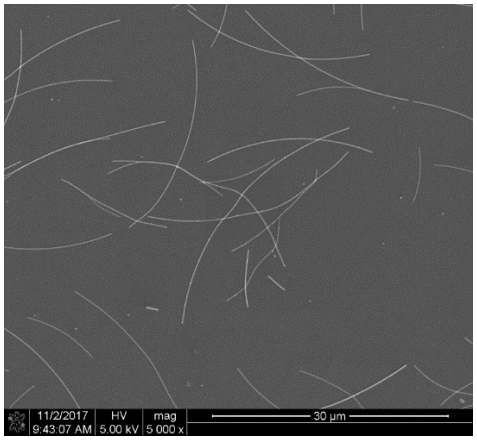
Flexible Ultra-short Channel Organic Ferroelectric Non-volatile Memory Transistors

Enlong Li,[1] *Xiaomin Wu,*[1] *Shuqiong Lan,*[1] *Qian Yang,*[1,2] *Yuan Fang,*[1] *Huipeng Chen*[1] ** and Tailiang Guo*[1]

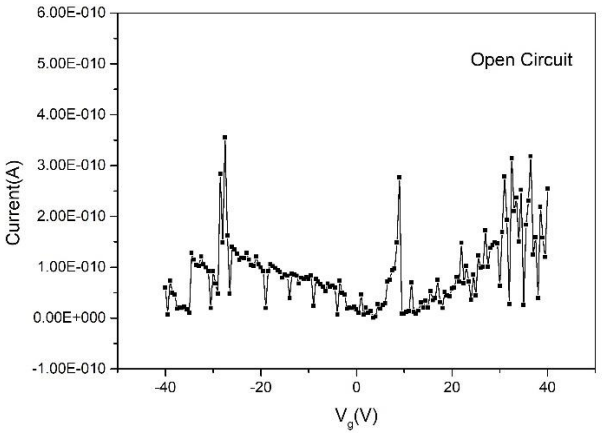
[1]Institute of Optoelectronic Display, National & Local United Engineering Lab of Flat Panel Display Technology, Fuzhou University, Fuzhou 350002, China
*Email: hpchen@fzu.edu.cn

[2]Zhicheng College, Fuzhou University, Fuzhou 350002, China

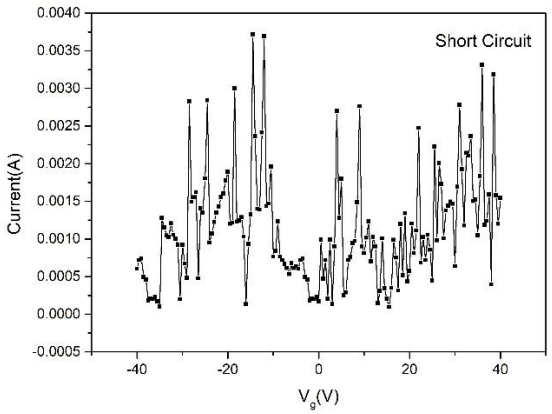
a）



b）



c）



d）

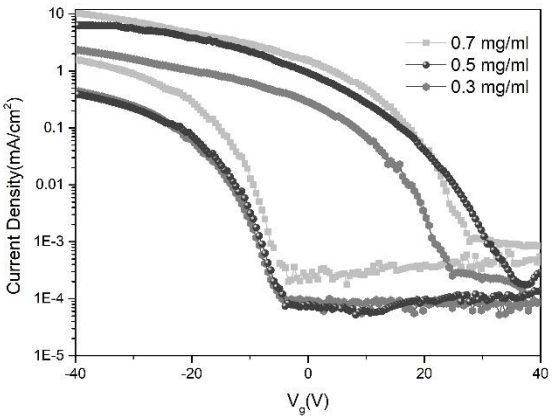


Figure S1. a）SEM image of 0.1 mg ml^{-1} Ag nanowires，b） and c）transfer curves of ferroelectric memory device based on 0.1 mg ml^{-1} Ag nanowires and 1 mg ml^{-1} Ag nanowires respectively，d）memory performance of ferroelectric memory devices based on 0.3 mg ml^{-1}, 0.5 mg ml^{-1}, and 0.7 mg ml^{-1} Ag nanowires，respectively. The pulse time was 1 s with constant $V_{P/E} = \pm 40$ V and V_{DS} at -40 V.

The SEM image exhibited that there were many vacant places without Ag nanowires，which meant that the Ag nanowires can hardly form mesh electrode resulting in open circuit as was shown in Figure S1b. In contrast，short circuit occurred when the concentration of Ag nanowires was 1 mg ml^{-1} and the result was shown in Figure S1c. The variation of transfer characteristic curves of ferroelectric memory devices based on 0.3 mg ml^{-1}, 0.5 mg ml^{-1}, and 0.7 mg ml^{-1} Ag nanowires respectively were presented in Figure S1d. The memory window and memory ratio were listed in Table S1, which indicated that the device based on 0.5 mg ml^{-1} Ag nanowires exhibited the best memory performance.

Table S1

Concentration of Ag nanowires	Memory window（V）	Memory ratio
0.3 mg ml^{-1}	30	1×10^3
0.5 mg ml^{-1}	38	7×10^3
0.7 mg ml^{-1}	33	1×10^3

a) b)

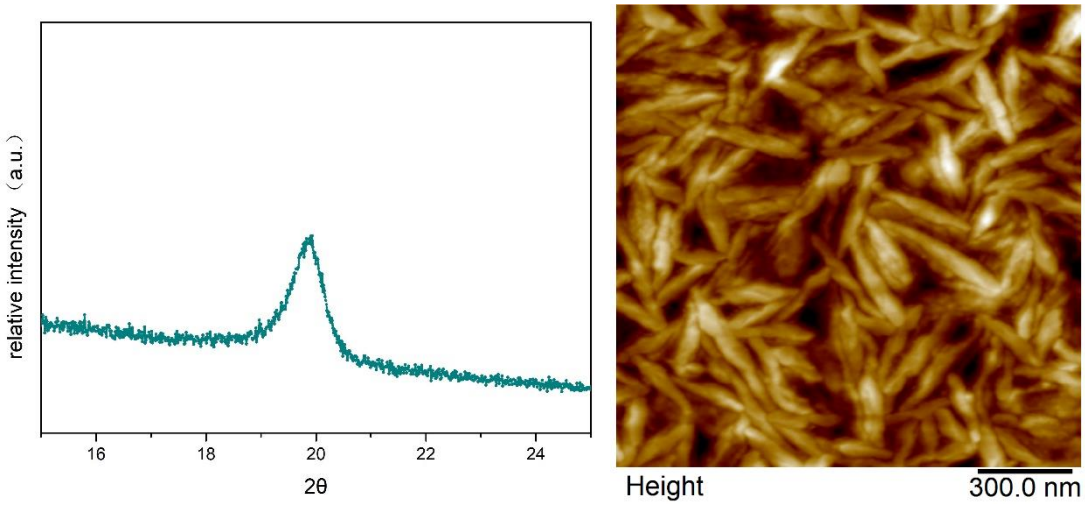


Figure S2. a）and b)the XRD and AFM images of P(VDF-Trfe) heating at 150° for 10 minutes which is the approximate time of deposited process after annealing.

The XRD showed the diffraction peak at 2θ=19.7° which is the characteristic of （200）and （110） crystalline planes of the ferroelectric β phase. A rough morphology consisting of a network of fiber-like structure can be observed in the AFM image in Figure S3b. The increasing temperature attributed to the fusion of neighboring grains into rods, resulting in the formation of long extended fiber-shaped crystals. Comparing with the AFM images at 130°， we can find that length of these rods increases with increasing annealing temperatures and this is consist with previous work[1,2,3].

Device Fabrication

For the fabrication of rigid ultra-short channel FeFET memory device, the Si wafer with 100nm SiO_2 was ulatrasonicated in acetone and isopropanol for 10 min respectively, and then dried with nitrogen. P(VDF-TrFE) was dissolved in dimethyformamide (DMF) in the ratio of 4 wt. % followed by stirring over 24 h to ensure complete dissolution. Then the film of P(VDF-TrFE) was formed by spin-coating at 4000rpm for 60s followed by soft baking at 80℃. The film was the annealing at 130℃ for 2h to gain the β phase of ferroelectric layer and enhance the crystallinity. 4nm Al_2O_3, working as a buffer layer to hold Ag nanowires (AgNws), was deposited by atomic layer deposition (ALD) under deposition temperature of 150°C, using trimethylaluminum (TMA) and water (H_2O) as the precursors and reactant respectively. To form the mesh source, AgNws solution was spin-coated on top of Al_2O_3 layer at 2000 rpm for 60 s and annealed at 100°C for 60 s in order to remove the residual isopropanol. A 50 nm gold source was thermally evaporated onto the AgNws through a sophisticated shadow mask. After that, the PDVT-8 film was coated on the substrate by spin-coating at 1000 rpm for 60 s and then annealed at 150 °C for 10 min. The thickness of active layer is about 120nm. To form a separate semiconductor layer, the sample was immersed in chloroform solvent to remove the excess PDVT-8 so that the deposited gold electrode will be completely exposed. Finally, 50 nm gold drain electrode was deposited through thermal evaporation as drain electrode. The effective channel area is determined by the overlapping area

between the AgNws and top gold drain electrode which is approximate 200um×200um. Detailed illustration of the rigid device preparation process flow diagram was presented in Figure S1. For the preparation of flexible memory device, the glass was used as bottom substrate and PI solution was deposited onto the glass substrate by blade coating with a blade gap of 100um. Subsequently annealed at 80 °C for 12 h, 120 °C for 1 h, 180 °C for 1 h, 250 °C for 1 h and 300 °C for 0.5 h inside a vacuum oven successively. Then 100 nm Al_2O_3 was deposited on the top of PI as the buffer layer by ALD. The bottom Al gate electrode was prepared by thermal evaporation followed by deposition of 100 nm Al_2O_3 as a blocking dielectric layer with the same ALD process conditions described above. The deposition of P(VDF-TrFE), AgNws, PDVT-8, and the source and drain electrodes were following the same process as the rigid device as mentioned above. Figure S1 showed the fabrication flow for a rigid FeFET non-volatile memory device.

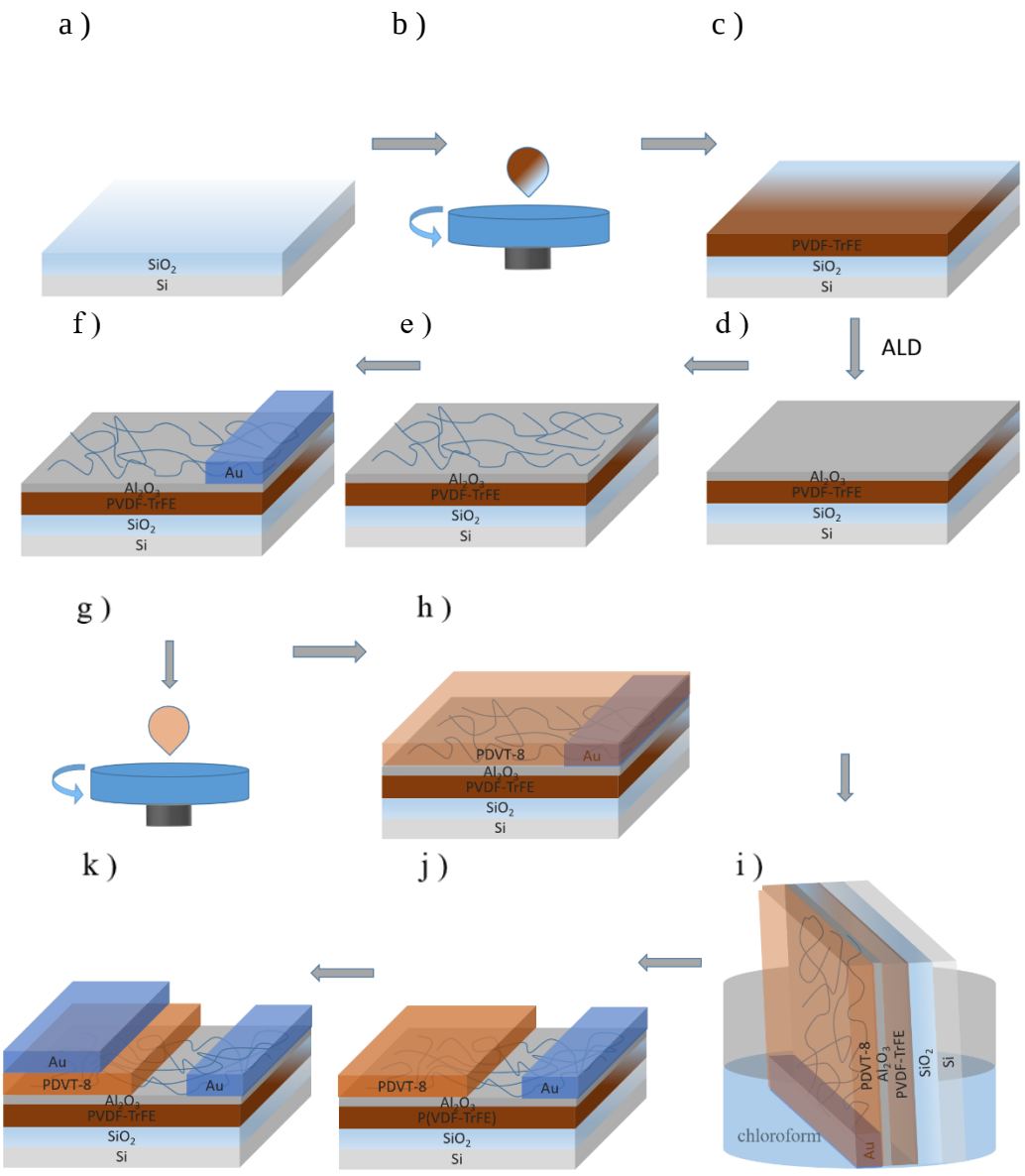


Figure S3. Schematic illustration of the fabrication flow for a rigid ultra-short channel FeFET non-volatile memory device a)， b）and c）spin coating of P(VDF-TrFE), d) deposition of Al_2O_3 buffer layer by atomic layer deposition (ALD), e) spin coating of AgNws to form mesh source, f) deposition of gold electrode by thermal evaporation using a sophisticated shadow mask, g and h）spin coating of PDVT-8, i）partially immersed the device in the chloroform solvent by a dip method to pattern

organic semiconductor layer, j) patterned organic semiconductor, k) thermally evaporated gold as drain electrode.

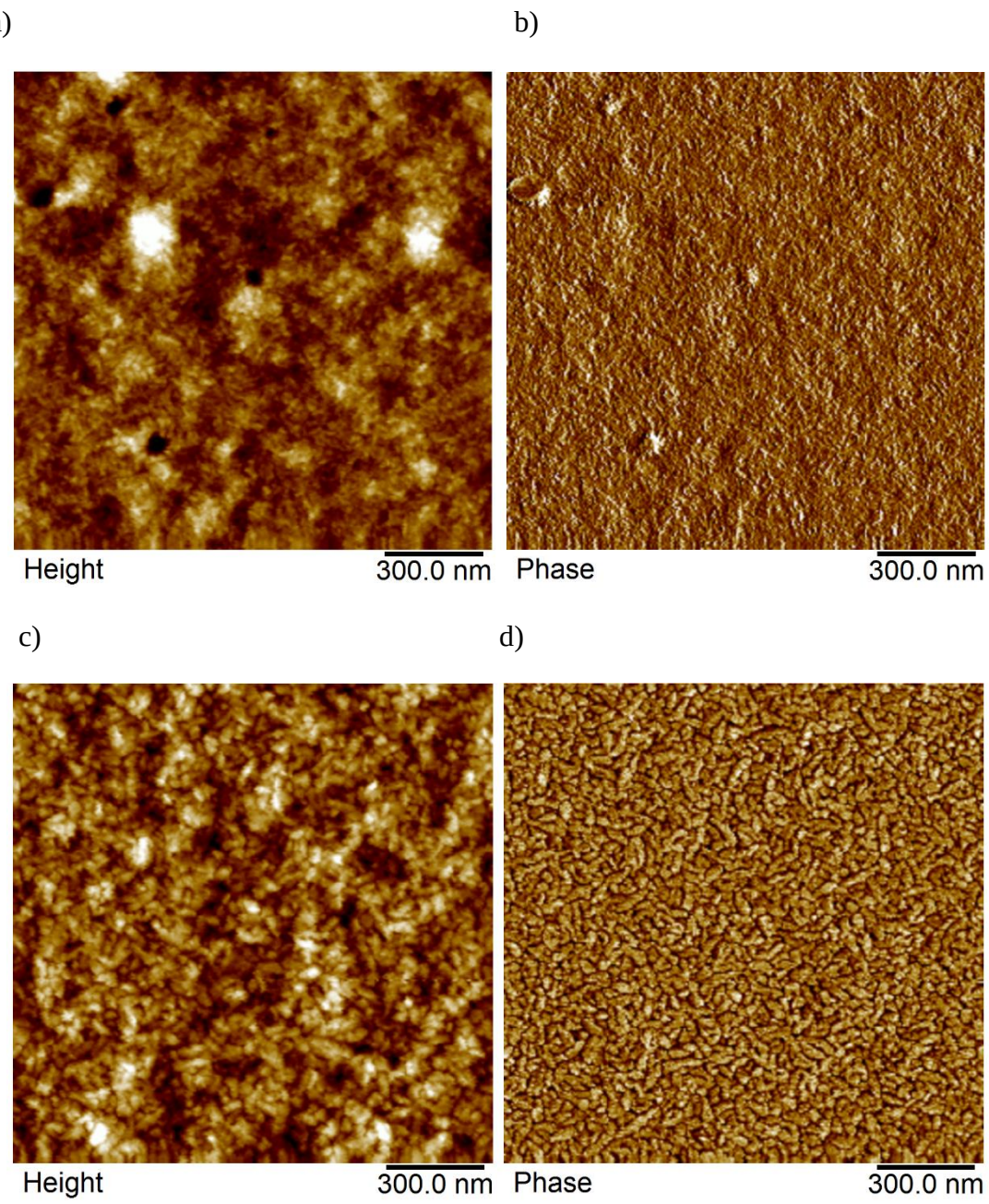


Figure S4. a) and b) the AFM images with height and phase mode, respectively of P(VDF-TrFE) before annealing, c) and d) the height and phase mode of P(VDF-TrFE) after a 80°C soft bake followed a 130°C annealing.

The ferroelectric film without annealing showed poor crystallinity, while after annealing significant improvement in crystallization and relatively larger roughness was observed.

References

1. G. Suresh, G. Mallikarjunachari, S. Jatav, C. Thirmal, M. S. R. Rao and D. K. Satapathy, *J Appl Polym Sci*, 2018, **135**. 45955
2. Li, W.; Zhu, Y.; Hua, D.; Wang, P.; Chen, X.; Shen, J. Appl. Surf. Sci. 2008, **254,** 7321
3. Li, W.; Yu, L.; Zhu, Y.; Hua, D.; Wang, J.; Luo, L.; Zhang, J. J. Appl. Polym. Sci. 2010, **116**, 663.