Supplementary Information

Fabrication of flexible high-performance organic field-effect transistors using phenacene molecules and their application toward flexible CMOS inverters

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Table S1. FET parameters of $(C_{14}H_{29})_2$-picene thin-film FET with parylene gate dielectric formed on 500 μm thick PET substrate. V_D = -100 V.

device	μ ($cm^2 V^{-1} s^{-1}$)	$\lvert V_{th} \rvert$ (V)	*ON/OFF*	*S* (V $decade^{-1}$)	*L* (μm)	*W* (μm)
#1	1.10	60.1	6.48×10^6	4.08	200	500
#2	7.56×10^{-1}	61.7	5.50×10^6	4.01	150	500
#3	4.61×10^{-1}	58.1	6.04×10^6	4.05	100	500
#4	2.35×10^{-1}	62.4	4.98×10^6	4.88	50	500
#5	1.34	58.3	3.16×10^5	11.1	285	500
#6	9.52×10^{-1}	62.3	5.04×10^6	4.61	200	500
#7	5.80×10^{-1}	59.5	5.27×10^6	3.51	135	500
#8	4.36×10^{-1}	63.0	4.45×10^6	4.18	100	500
#9	1.58×10^{-1}	56.1	4.56×10^6	3.55	50	500
average	$7(4) \times 10^{-1}$	60(2)	$5(2) \times 10^6$	5(2)		

Table S2. FET parameters of $(C_{14}H_{29})_2$-picene thin-film FET with parylene gate dielectric formed on 125 μm thick PET substrates. V_D = -100 V.

device	μ ($cm^2 V^{-1} s^{-1}$)	$\lvert V_{th} \rvert$ (V)	*ON/OFF*	*S* (V $decade^{-1}$)	*L* (μm)	*W* (μm)
#1	3.64×10^{-1}	62.7	1.40×10^{6}	4.62	250	500
#2	1.82×10^{-1}	61.8	1.35×10^{6}	6.32	135	500
#3	3.28×10^{-1}	63.0	1.25×10^{6}	7.50	250	500
#4	2.07×10^{-1}	62.2	1.02×10^{6}	6.01	200	500
#5	2.76×10^{-1}	65.1	9.32×10^{5}	6.73	250	500
#6	1.23×10^{-1}	62.7	8.72×10^{5}	4.73	135	500
#7	2.51×10^{-1}	64.5	8.76×10^{5}	5.42	250	500
#8	3.98×10^{-1}	64.1	1.01×10^{6}	6.27	350	500
#9	7.01×10^{-1}	62.4	1.51×10^{6}	5.00	600	500
average	$3(2) \times 10^{-1}$	63(1)	$1.1(2) \times 10^{6}$	6(1)		

Table S3. FET parameters of $(C_{14}H_{29})_2$-picene thin-film FET with ZrO_2 gate dielectric formed on 125 µm thick PET. V_D = -16V.

device	μ ($cm^2 V^{-1} s^{-1}$)	$\lvert V_{th} \rvert$ (V)	*ON/OFF*	*S* (V $decade^{-1}$)	*L* (µm)	*W* (µm)
#1	8.34×10^{-1}	8.07	8.97×10^4	1.30	50	300
#2	1.49	8.01	6.67×10^4	1.33	100	300
#3	8.96×10^{-1}	8.90	4.37×10^4	1.40	80	300
#4	5.12	6.25	1.75×10^5	1.25	450	880
average	2(2)	8(1)	$9(6) \times 10^4$	1.32(6)		

Table S4. FET parameters of $(C_{14}H_{29})_2$-picene thin-film FET with ZrO_2 gate dielectric formed on 350 μm thick PET. V_D = -16V.

device	μ ($cm^2 V^{-1} s^{-1}$)	$\lvert V_{th} \rvert$ (V)	*ON/OFF*	*S* (V $decade^{-1}$)	*L* (μm)	*W* (μm)
#1	4.14	6.47	1.60×10^6	9.91×10^{-1}	250	500
#2	4.18	5.09	7.15×10^6	9.69×10^{-1}	250	500
#3	1.25	6.74	1.21×10^6	8.58×10^{-1}	450	500
#4	0.88	6.61	4.87×10^5	1.08	250	500
#5	6.31	6.6	9.79×10^7	1.07	600	500
#6	2.78	7.44	1.67×10^5	1.14	450	500
#7	4.14	5.89	5.00×10^5	1.11	250	500
average	3(2)	6.4(7)	$2(4) \times 10^7$	1.0(1)		

Table S5. FET parameters of FET parameters of [6]phenacene thin-film FET with parylene gate dielectric formed on 125 μm thick PET substrates. V_D = -120 V.

device	μ ($cm^2 V^{-1} s^{-1}$)	$\lvert V_{th} \rvert$ (V)	*ON/OFF*	*S* (V $decade^{-1}$)	*L* (μm)	*W* (μm)
#1	2.11×10^{-1}	60.7	5.28×10^{4}	6.20	350	500
#2	1.65×10^{-1}	58.7	1.13×10^{6}	2.48	450	1000
#3	1.80×10^{-1}	61.2	3.08×10^{6}	1.71	450	1000
#4	2.03×10^{-1}	59.5	9.45×10^{4}	2.92	450	1000
average	$1.9(2) \times 10^{-1}$	60(1)	$1(1) \times 10^{6}$	3(2)		

Table S6. FET parameters of FET parameters of [6]phenacene thin-film FET with parylene gate dielectric formed on 350 μm thick PET substrates. V_D = -120 V.

device	μ ($cm^2 V^{-1} s^{-1}$)	$\lvert V_{th} \rvert$ (V)	*ON/OFF*	*S* (V $decade^{-1}$)	*L* (μm)	*W* (μm)
#1	7.00×10^{-2}	58.1	1.93×10^4	7.15	100	300
#2	1.47×10^{-1}	57.1	2.58×10^4	6.25	450	1000
#3	2.23×10^{-1}	55.2	5.37×10^4	5.94	450	1000
#4	2.10×10^{-1}	53.9	2.10×10^6	2.05	450	1000
average	$1.6(7) \times 10^{-1}$	56(2)	$1(1) \times 10^5$	5(2)		

Table S7. FET parameters of FET parameters of [6]phenacene thin-film FET with parylene gate dielectric formed on 500 μm thick PET substrates. V_D = -120 V.

device	μ ($cm^2 V^{-1} s^{-1}$)	$\lvert V_{th} \rvert$ (V)	*ON/OFF*	*S* (V $decade^{-1}$)	*L* (μm)	*W* (μm)
#1	1.49×10^{-1}	59.9	1.23×10^{5}	6.14	350	500
#2	2.24×10^{-1}	58.0	2.48×10^{5}	5.71	450	1000
#3	1.56×10^{-1}	57.4	1.92×10^{5}	6.16	450	1000
#4	9.70×10^{-2}	61.7	7.50×10^{4}	6.31	450	500
#5	2.55×10^{-1}	58.4	1.16×10^{5}	6.68	600	500
#6	7×10^{-2}	62.8	2.54×10^{4}	7.13	600	500
average	$1.6(7) \times 10^{-1}$	60(2)	$1.3(8) \times 10^{5}$	6.4(5)		

Table S8. FET parameters of PTCDIC8 thin-film FET with parylene gate dielectric formed on 125 μm thick PET. V_D =100V

device	μ ($cm^2 V^{-1} s^{-1}$)	V_{th} (V)	*ON/OFF*	*S* (V $decade^{-1}$)	*L* (μm)	*W* (μm)
#1	2.43×10^{-2}	70.9	1.99×10^3	18.5	100	300
#2	6.62×10^{-2}	62.8	4.55×10^3	12.6	285	500
#3	3.05×10^{-2}	68.5	7.31×10^3	11.5	450	1000
#4	2.28×10^{-2}	70.4	5.08×10^3	16.6	450	1000
#5	3.88×10^{-2}	64.7	3.08×10^3	12.9	450	1000
#6	7.56×10^{-2}	54.6	4.00×10^3	13.3	600	500
average	$4(2) \times 10^{-2}$	65(6)	$4(2) \times 10^3$	14(3)		

Table S9. FET parameters of PTCDIC8 thin-film FET with parylene gate dielectric formed on 500 μm thick PET substrates. V_D =100V.

device	μ ($cm^2 V^{-1} s^{-1}$)	V_{th} (V)	*ON/OFF*	*S* (V $decade^{-1}$)	*L* (μm)	*W* (μm)
#1	7.85×10^{-2}	67.3	5.32×10^3	17.0	100	300
#2	1.67×10^{-1}	59.7	6.88×10^3	15.8	450	1000
#3	1.44×10^{-1}	48.9	9.17×10^3	13.8	450	1000
#4	8.32×10^{-2}	61.3	8.67×10^3	15.3	450	1000
#5	1.65×10^{-1}	58.9	5.73×10^3	16.7	600	500
#6	1.82×10^{-1}	60.4	5.56×10^3	16.8	600	500
average	$1.4(4) \times 10^{-1}$	59(6)	$7(2) \times 10^3$	16(1)		

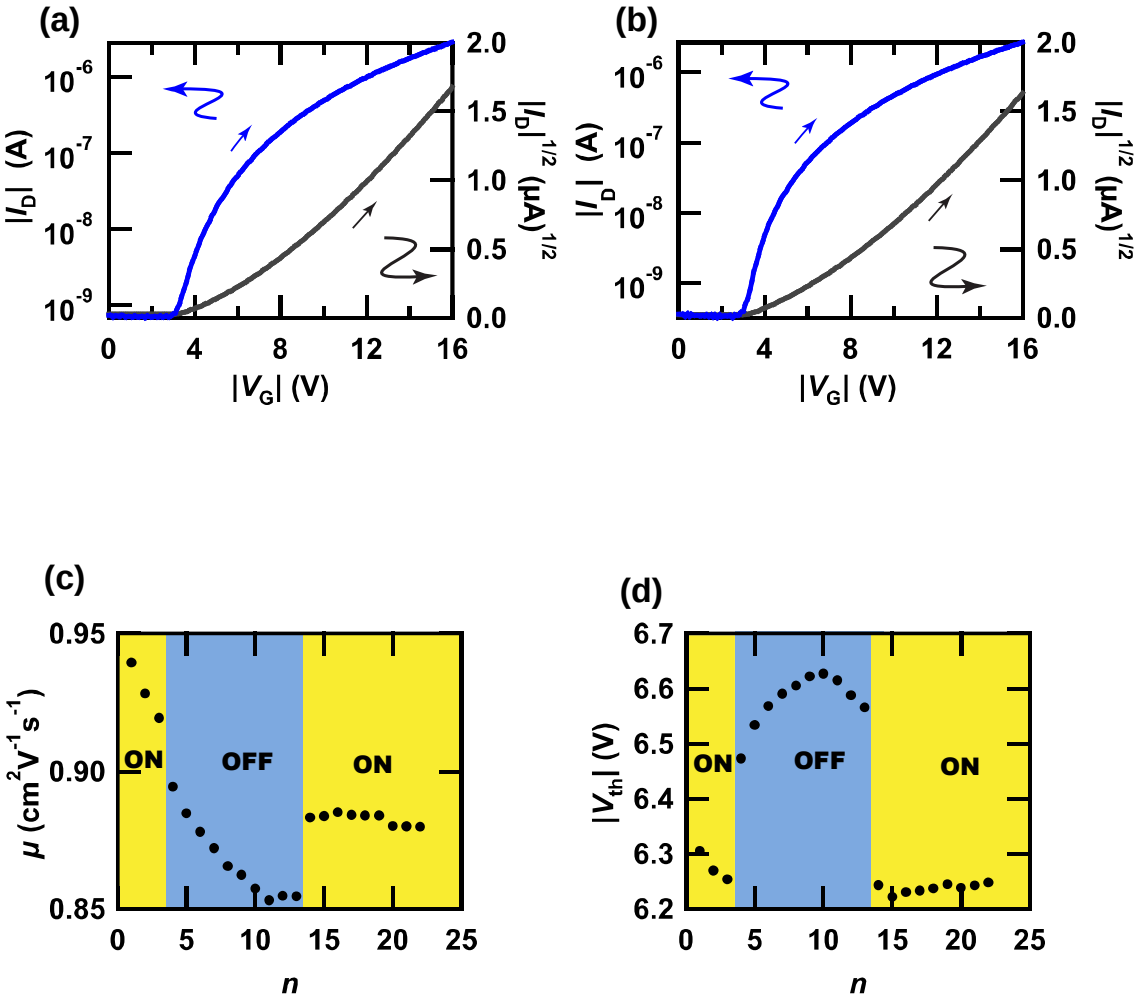

Figure S1. (a) Forward transfer curves in 1st and (b) 22nd measurements, and plots of (c) μ – n, (d) $|V_{th}|$ - n in [6]phenacene thin-film FET with ZrO_2 gate dielectric formed on 125 μm thick PEN. The device structure is the same as that shown in Figure 7(a).

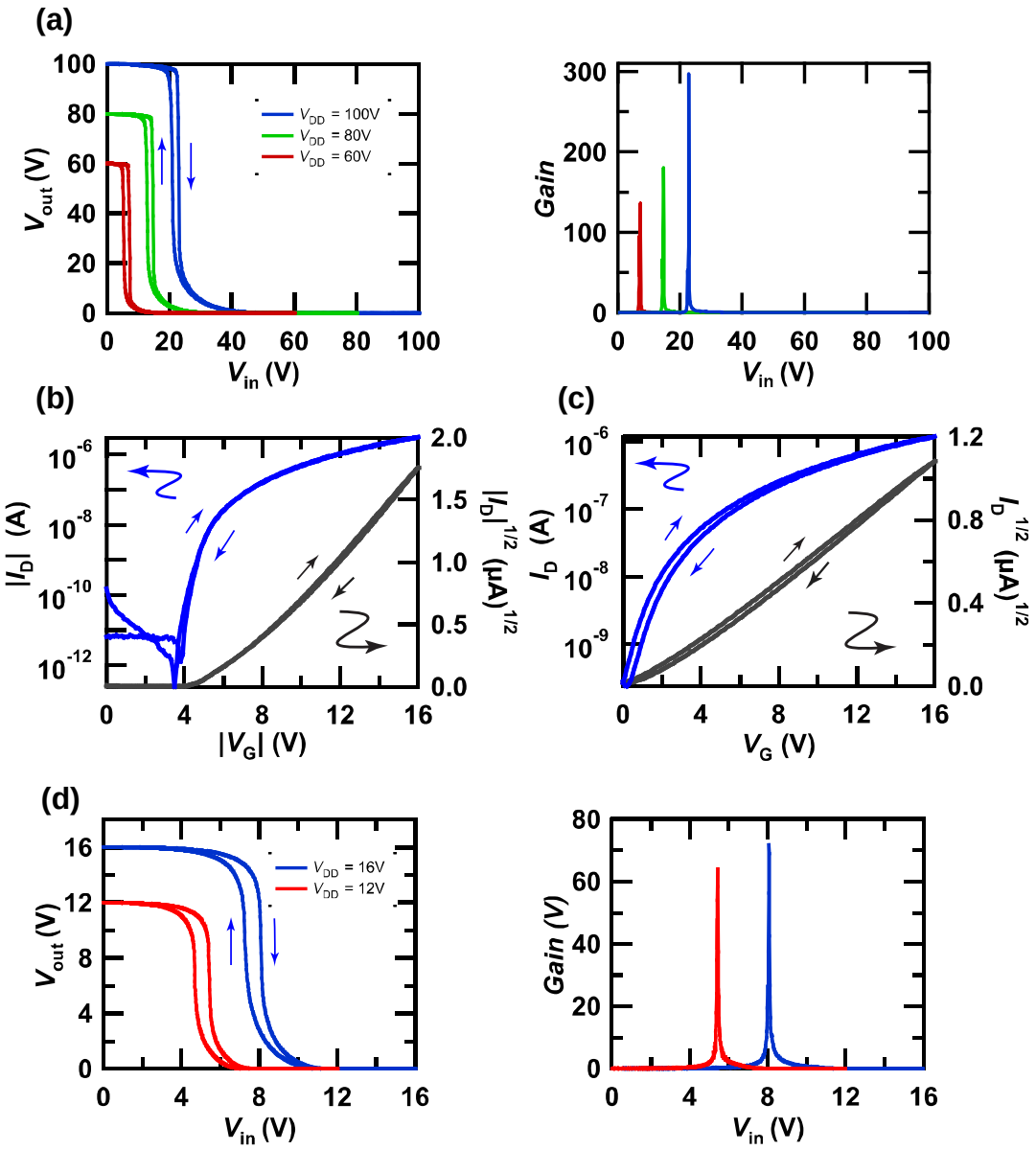

Figure S2. (a) Plots of V_{out} – V_{in} and gain – V_{in} in [6]phenacene / PTCDIC8 CMOS inverter formed on 125 μm thick PEN. Parylene was used for gate dielectric. (b) Transfer curve of [6]phenacene thin-film FET and (c) transfer curve of PTCDIC8 thin-film FET. These devices were made on 125 μm thick PEN, which constitute the CMOS inverter. ZrO_2 was used for gate dielectric. (d) Plots of V_{out} – V_{in} and gain – V_{in} in the [6]phenacene / PTCDIC8 CMOS inverter which is composed of FETs shown in (b) and (c). Both forward and reverse V_{out} – V_{in} plots are drawn in (a) and (d), while only a forward gain – V_{in} plot is shown in (a) and (d).