

Electronic Supplementary Information

Parylene Copolymer Gate Dielectrics for Organic Field-Effect Transistors

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Experimental Details

Materials: The parylene C (diX-C, Daisankasei Co., Ltd.) and F (VT4, Suzhou Chireach Biomedical Technology Co., LTD.) were prepared for gate dielectrics. For the bank solution, Cytop (CTL-809M, Asahi Glass) was dissolved in fluorinate solvent (CT-Solv.180, Asahi Glass) at a volume ratio of 1:2. The semiconductor solution was prepared with a blend of 2.5 mg ml⁻¹ TIPS-pentacene (>99.9 %, Ossila) and 1.25 mg ml⁻¹ polystyrene (PS) (M_w ~280,000, Sigma-Aldrich) dissolved in mesitylene (98 %, Sigma-Aldrich).

Characterization: The concentration of chlorine and fluorine atoms was measured by SIMS (IMS 6F, Cameca). The thickness of parylene thin films was measured using a stylus surface profiler (DektakXT, Bruker). The capacitance of MIM capacitors was measured with a precision LCR meter (ZM2376, NF Corporation) within the frequency range of 1 Hz to 1 MHz. The electrical characteristics of OFETs were measured with a semiconductor parameter analyzer (4200-SCS, Keithley) under ambient conditions inside a dark box. AFM images were recorded in tapping mode using an SPM system (Veeco Dimension 3100 + Nanoscope V, Digital Instruments/Veeco Metrology Group). The crystalline of TIPS-pentacene thin films was recorded by POM (Leica DM2700M, Leica). 2D GIXRD measurements were performed at the 3C beamline ($\lambda = 1.37 \text{ \AA}$) of the Pohang Acceleration Laboratory in Korea.

OFET Fabrication: BGTC OFETs were fabricated on glass substrates (Eagle XG, Corning). A 50 nm thick aluminum gate electrode was thermally evaporated through a shadow mask on the substrate. The parylene gate dielectric was deposited by means of CVD. The temperature of the vaporizer was maintained at 65 and 75 °C for 30 min in each step. During CVD, the temperature

of the pyrolysis furnace was maintained at 690 °C to decompose of parylene dimers to monomers. Cytop solution was printed using a dispenser (350PC, Musashi Engineering, Inc.) to form the bank, followed by thermal annealing at 100 °C for 10 min on a hotplate to remove residual solvent. The substrate and nozzle temperatures were maintained at 40 °C during the dispenser patterning process. The semiconductor solution was printed onto the area defined by the banks using the dispenser, followed by thermal annealing at 70 °C for 10 min on a hotplate for crystallization of TIPS-pentacene thin film and removal of residual solvent. The substrate and nozzle temperatures were maintained at 30 °C during the dispenser patterning process. Finally, a 40 nm thick silver was thermally evaporated through a shadow mask for source and drain electrodes with channel width and length of 1000 and 50 μm , respectively.

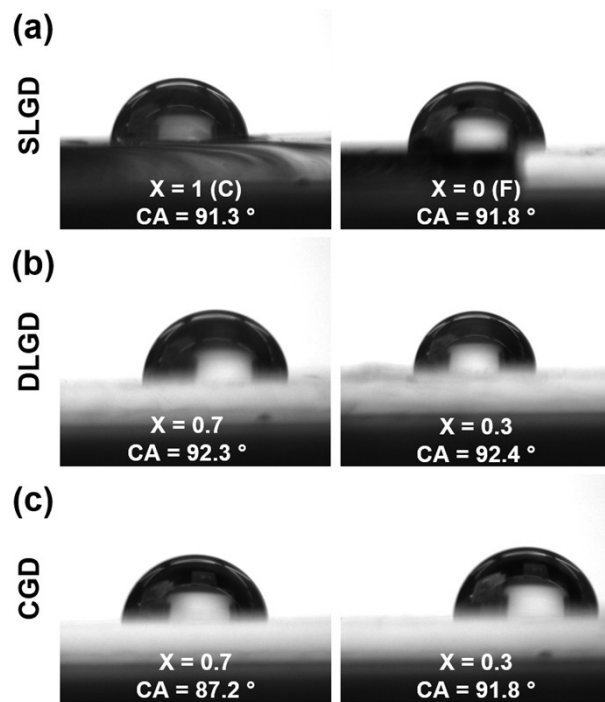


Fig. S1 Contact angle of DI water prepared on parylene (a) SLGDs, (b) DLGDs, and (c) CGDs.

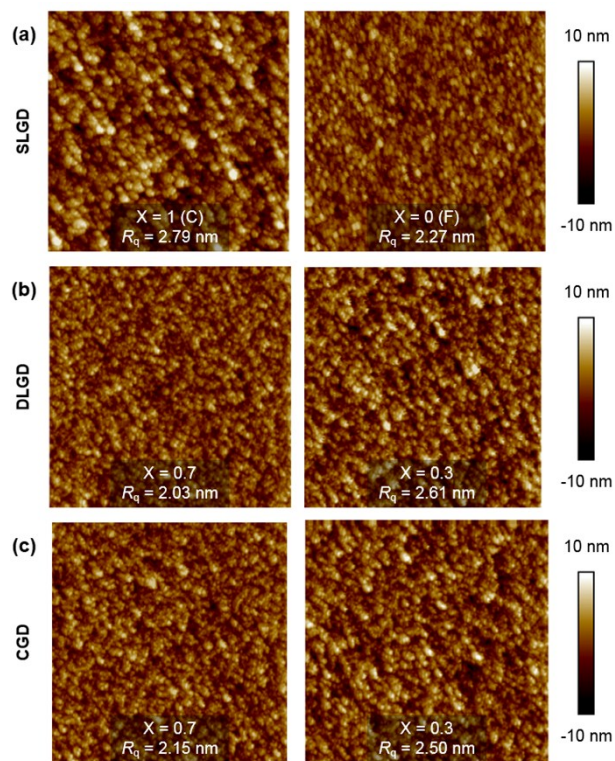


Fig. S2 AFM images of parylene (a) SLGDs, (b) DLGDs, and (c) CGDs in an area of $5 \mu\text{m} \times 5 \mu\text{m}$.

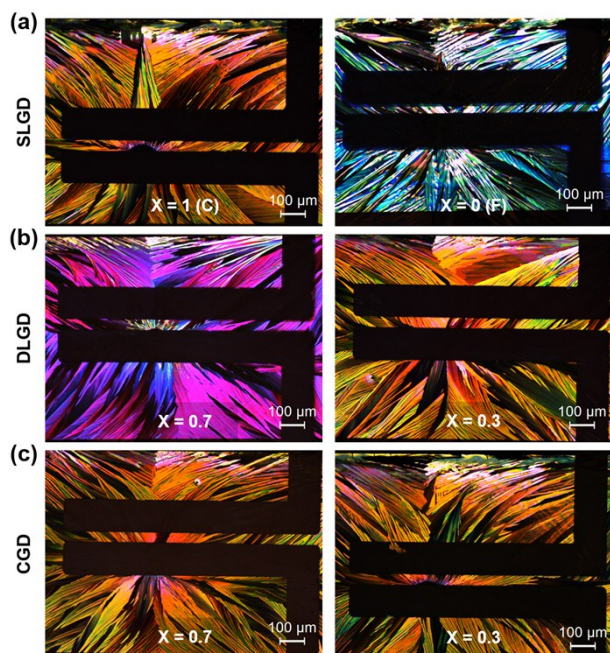


Fig. S3 POM images of TIPS-pentacene thin films deposited on parylene (a) SLGDs, (b) DLGDs, and (c) CGDs.

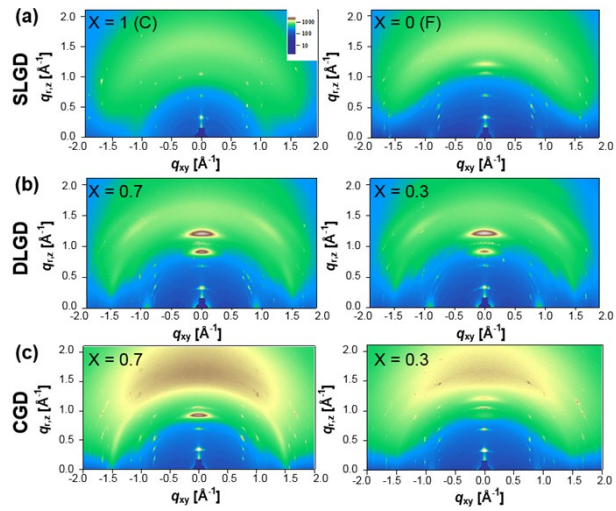


Fig. S4 2D GIXRD patterns of TIPS-pentacene thin films deposited on parylene (a) SLGDs, (b) DLGDs, and (c) CGDs.

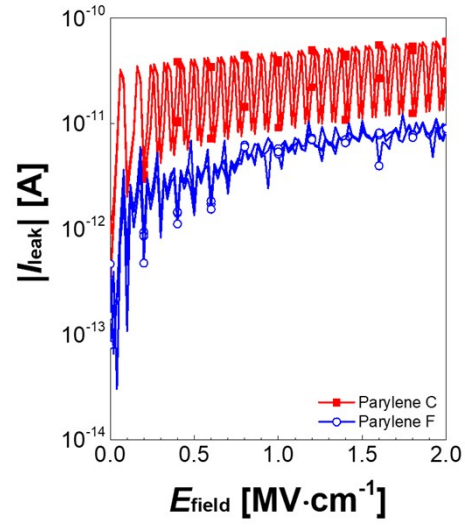


Fig. S5 Leakage currents of MIM capacitors using parylene C (red solid symbols) and F (blue open symbols) thin films.

Table S1 Dielectric and electrical parameters of parylene SLGDs, DLGDs, and CGDs.

$X =$ $w_C (w_C + w_F)^{-1}$	t_d [nm]	ϵ_r at 10 Hz	μ_{FET} [cm ² V ⁻¹ s ⁻¹]	E_{TH} [MV cm ⁻¹]	SS [V decade ⁻¹]	I_{on}/I_{off} [$\times 10^6$]	
SLGD	1 (C)	162	3.73	0.14 \pm 0.03	-0.11 \pm 0.01	0.43 \pm 0.22	15.6 \pm 23.39
	0 (F)	119	2.12	0.06 \pm 0.01	-0.15 \pm 0.04	2.59 \pm 1.17	1.82 \pm 1.05
DLGD	0.7	226	3.32	0.13 \pm 0.04	-0.08 \pm 0.01	0.55 \pm 0.45	4.90 \pm 2.34
	0.5	284	2.99	0.12 \pm 0.02	-0.10 \pm 0.01	0.65 \pm 0.37	6.27 \pm 4.01
	0.3	219	2.64	0.05 \pm 0.01	-0.13 \pm 0.02	2.24 \pm 0.64	3.34 \pm 3.05
CGD	0.7	175	3.11	0.13 \pm 0.01	-0.10 \pm 0.01	0.72 \pm 0.64	7.50 \pm 4.18
	0.5	262	2.92	0.14 \pm 0.03	-0.11 \pm 0.01	0.81 \pm 0.45	5.83 \pm 4.69
	0.3	183	2.44	0.14 \pm 0.03	-0.11 \pm 0.01	1.27 \pm 0.82	4.94 \pm 2.44

* $V_{TH} = E_{TH} \times t_d$

* Averaged over ten devices.

Table S2 The τ and β for OFETs with parylene SLGDs, DLGDs, and CGDs.

$X = w_C (w_C + w_F)^{-1}$		$\tau [\times 10^4 \text{ s}]$	β
SLGD	1 (C)	10.2 ± 1.4	0.65 ± 0.03
	0 (F)	5.9 ± 0.8	0.39 ± 0.01
DLGD	0.7	7.2 ± 2.6	0.55 ± 0.05
	0.5	11.2 ± 5.3	0.43 ± 0.04
	0.3	10.3 ± 1.7	0.37 ± 0.02
CGD	0.7	9.7 ± 3.0	0.72 ± 0.06
	0.5	10.3 ± 2.8	0.71 ± 0.03
	0.3	9.1 ± 1.4	0.65 ± 0.01

* Averaged over five devices.