Electronic Supplementary Information:

A. Capex and Cost per Unit Area

The historical data of cost and capex per area PV modules shows the decreasing trend over the years in Figure S1. The per-area cost and capex decouple the effect of module efficiency. The benchmark module efficiencies are 14% in 2010, 17% in 2015, and 19% in 2018. Despite the efficiency improvement, the cost and capex for cell and module processing are kept decreasing. The exponentially fitted trendlines extrapolate the decreasing trend to the future, although the decreasing rate will be slower. This indicates that it is likely to require the new technology to have cheaper processing cost and capex to gain sufficient market traction.

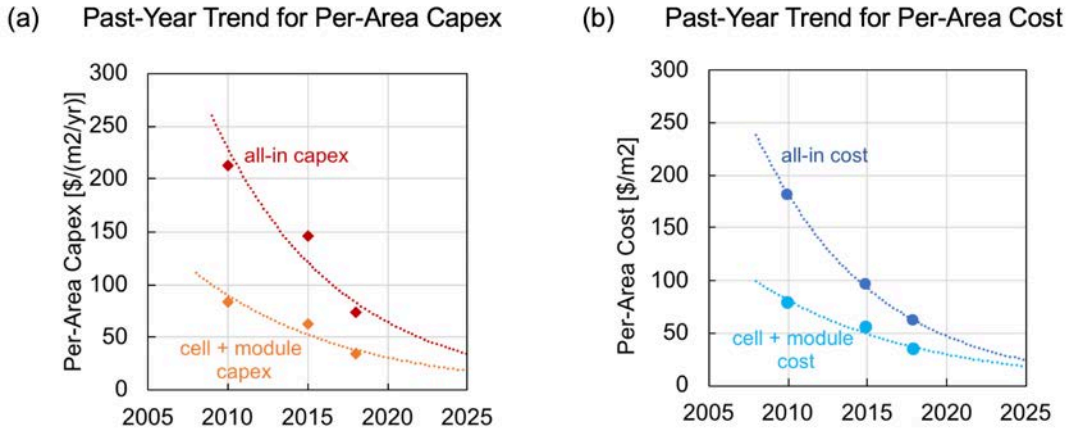

Figure S1: The decreasing trend for per-area capex and cost *versus* years. The capex and cost of the cell and module processes are shown separately in comparison with the all-in capex and cost. The dashed lines are the data trendlines with exponential fitting.

The per-area capex and cost values *versus* the wafer thickness is shown in Figure S2, which directly shows the cost change due to the savings from reducing silicon usage (regardless of the module efficiencies). The cost structure corresponding to the production process of the current PERC modules. We see capex reduction rate is \$2.3/(m^2/year) for reducing every 10 μm Si thickness, whereas cost reduction rate is \$1.2/m^2 for reducing every 10 μm Si thickness.

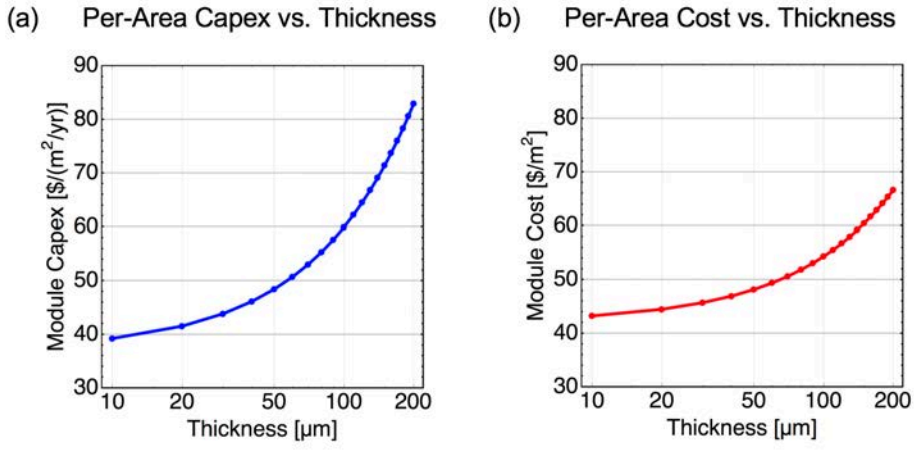

Figure S2: Per-area capex and cost versus silicon wafer thickness, which decoupled the effect of module efficiency.

B. Device Simulation Parameters

The simulation parameters for *p*-type PV modules are shown in Table S1, and the *I-V* characteristics of the *p*-type solar cells in Figure S3. To compare with the *p*-type PV modules in Figure 2, we also simulated the *n*-type module efficiency in Figure S4.

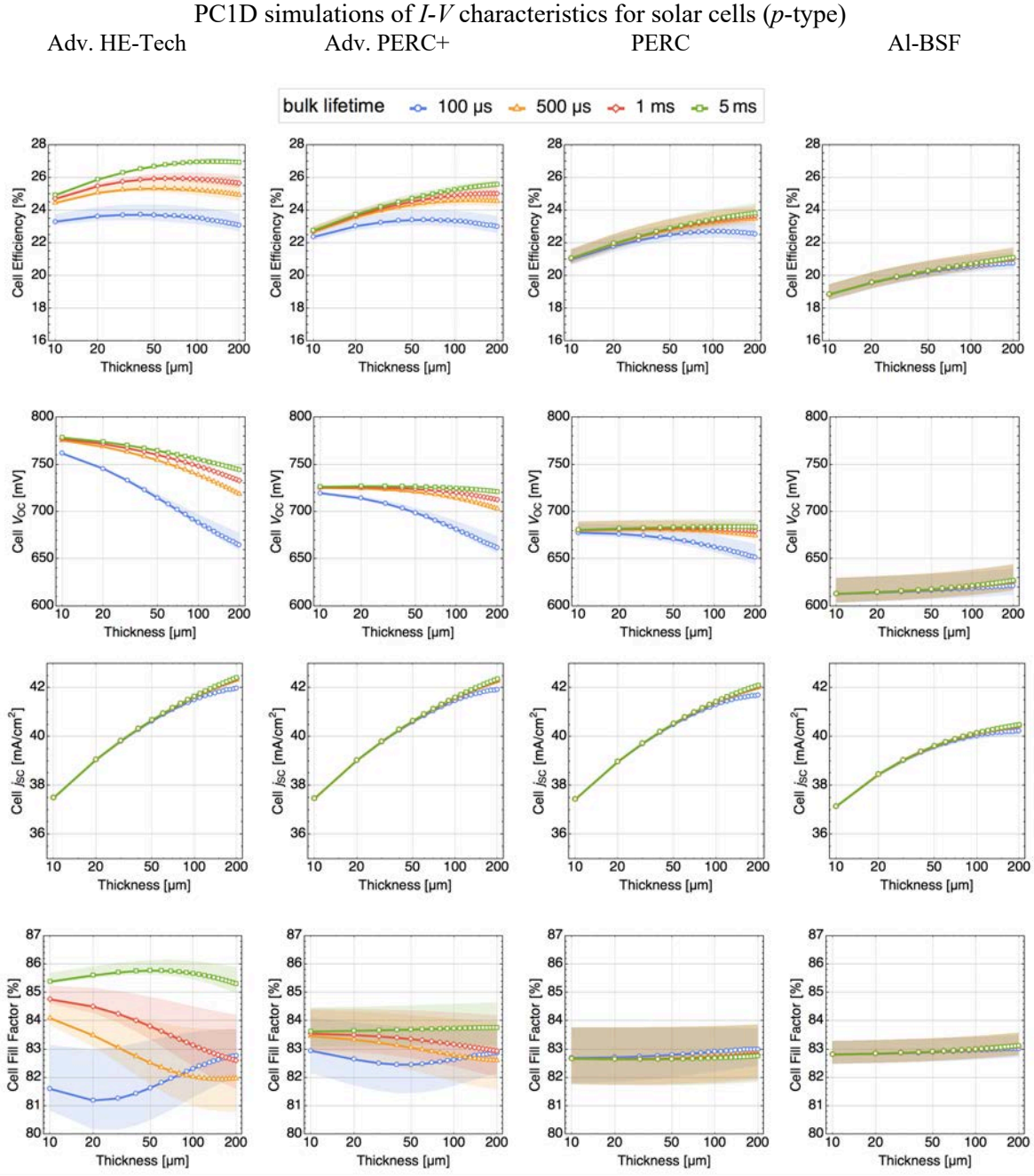

Figure S3: Solar cell efficiency, short-circuit current density j_{SC}, open-circuit voltage $V_{OC,}$ and fill factor *FF* for solar cells with different technology concepts with *p*-type wafers.

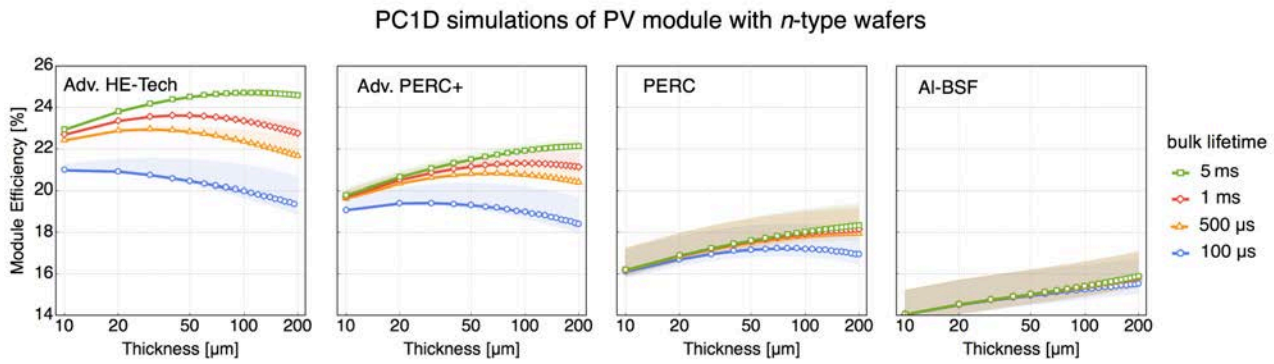

Figure S4: Simulated module efficiency with n-type wafers for different technological concepts and wafer bulk lifetimes. Base doping of *n*-type wafer is around 3 Ω·cm, with a typical range of 1 – 10 Ω·cm. The other parameters are set as the same as the p-type wafers in Table S1.

Table S1. Key parameters for PC1D device simulation of the four PV concepts in this study

Simulation Parameters	**Adv. HE-Tech**	**Adv. PERC+**	**PERC**	**Al-BSF**
Base resistivity, ρ_{base}	2 Ω·cm (*p*-type with a typical range of 1 – 3 Ω·cm)			
Emitter peak doping, N_{em}	6×10^{18} cm^{-3}	6×10^{19} cm^{-3}		
Front surface SRV, S_{front}	100 cm/s	1000 cm/s		
Rear surface SRV, S_{rear}	1 cm/s	10 cm/s	100 cm/s	1000 cm/s
Rear surface reflectance, R_b	93%			65%
Cell-to-module (CTM) efficiency factor, f_{CTM}	0.92	0.88	0.83	0.83
Concept characteristics	• Ultra-low front and rear SRV • Low Auger recombination • Ultra-low CTM efficiency loss	• Very low rear SRV • Very low CTM efficiency loss	• Low rear SRV • Low CTM efficiency loss	• High rear SRV • High parasitic absorption at the rear surface • High CTM efficiency loss

C. Technoeconomic Analysis of Two Different Scenarios

The capex and cost of solar cell processing steps may increase for advanced concepts, due to the increase process complexity. We investigate a scenario where 1.5x capex and cost increase in cell processing of advanced PERC+ and 2.0x capex and cost increase in solar cell processing of advanced HE-Tech. Note that the capex of cell processing is 30% of the total current capex and the cost of celling processing is 19% of the total current cost (see Figure 1). In such a scenario shown in Figure S5a below, the cost curves for all the technological concepts are more or less overlap with each other, and the effect of the cost increase is thickness-invariant. However, the capex curves for advanced concepts shift above the baseline PERC scenario due to the relatively large proportion of capex required in the cell processing step. In addition, the decreasing thickness reduces the overall capex proportion of poly-Si and wafer capex, and therefore the capex gaps between advance concepts and PERC are dominated by the cell processing capex. As an consequence of cost increase, the LCOE curves shifts up as well as compared to Figure 3. However, even though all three cost curves are overlapped, we still observed LCOE reductions for advanced concepts due to the benefit of efficiency improvement.

Although we see a continuous decease of kerf loss in the past years, there is still a chance that the kerf loss starts to become thickness invariant (*e.g.*, due to technology limitation of wire sawing process).

In the second scenario shown in Figure S5b, we investigate constant 95 µm thick silicon kerf loss for all wafer thicknesses. Effectively, the thickness-invariant kerf loss results in less silicon saving per wafer for thinner wafer, and kerf loss starts to dominate the silicon usage for the thickness below 95 µm. We see the capex and cost curves get flattened (as compared to Figure 3) due to this effect, and the potential savings by thin wafers get much reduced. However, we still observe the optimum thicknesses for capex, cost and LCOE are located around 50 µm or less.

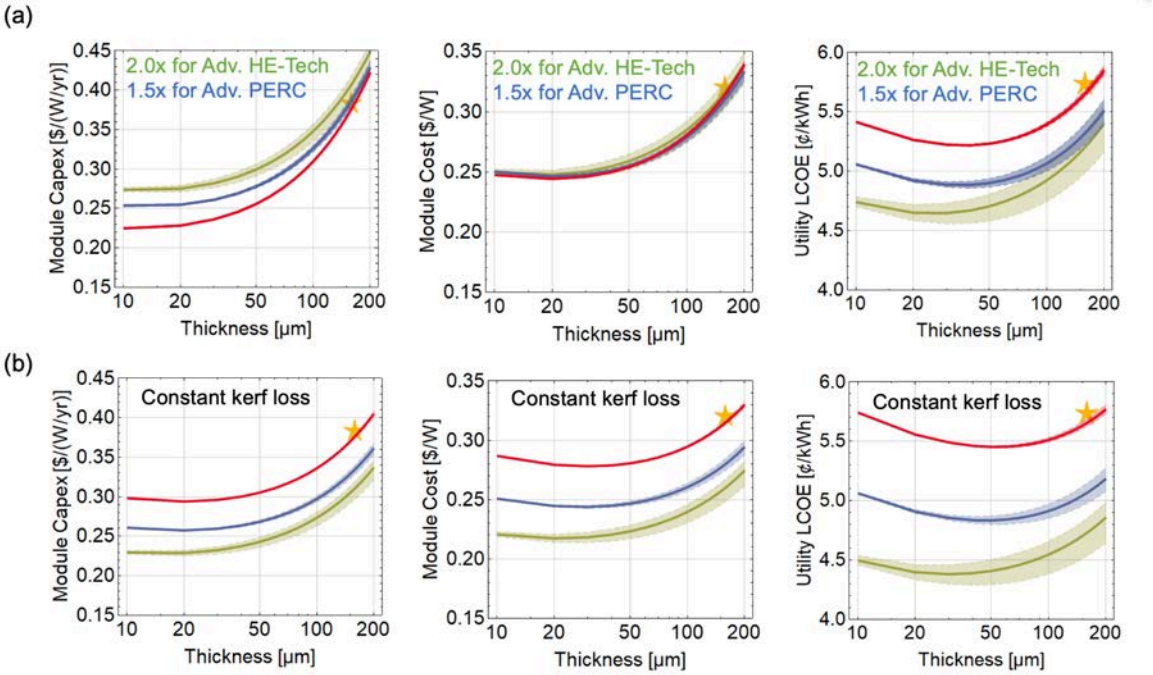

Figure S5: Cost analysis of two different scenarios: (a) capex and cost increase of cell processing of advanced concepts; (b) constant kerf loss of 95 µm thick silicon for all wafer thicknesses.

D. Maximum Sustainable Growth over Years

Large increases in renewable energy generation are needed by 2030 to maximize the probability of maintaining global temperatures less than 1.5 – 2°C above pre-industrial levels. Due to the current and projected costs of PV, it is expected that PV will have a large role to play in producing this low-carbon energy, with deployment targets in multi-terawatt scale by 2030 [1]. In particular, the IPCC has stated that renewable energy generation must represent 20–30% of the total energy generation in 2030 to have a 25–75% chance of keeping atmospheric CO_2 between 430–480 ppm. If one third of this generation comes from PV with an average capacity factor of 20%, then based on International Energy Agency projections of global energy demand [2], the total of 7–10 TW PV needs to be deployed by 2030. To achieve this target, the manufacturing capacity must expand at a cumulative annual growth rate of 22–25%. The possibility of achieving the IPCC 2030 climate targets for the advanced concepts in thin silicon wafers was evaluated.

In Figure S6a, current baseline PERC with 160 µm wafer will not lead us to the 2030 goal in various scenarios. High debt ratio accelerates PV deployment in the short term and get us closer to the 7 TW by 2030, however the long-term growth for all the scenarios reaches a plateau around 7 TW due to demand constraint. In Figure S6b, the advanced HE-tech with 160 µm wafer (*i.e.*, no thickness reduction) has a faster growth but a similar trend for the baseline PERC. It also moves the plateau point above 10 TW. Because of very significant capex and cost reduction in advanced HE-Tech with 50 µm wafer, the cumulative PV deployment in Figure S6c maintains exponential growth well beyond 10 TW (the plateau point for this case is around 25 TW, and not shown in this figure).

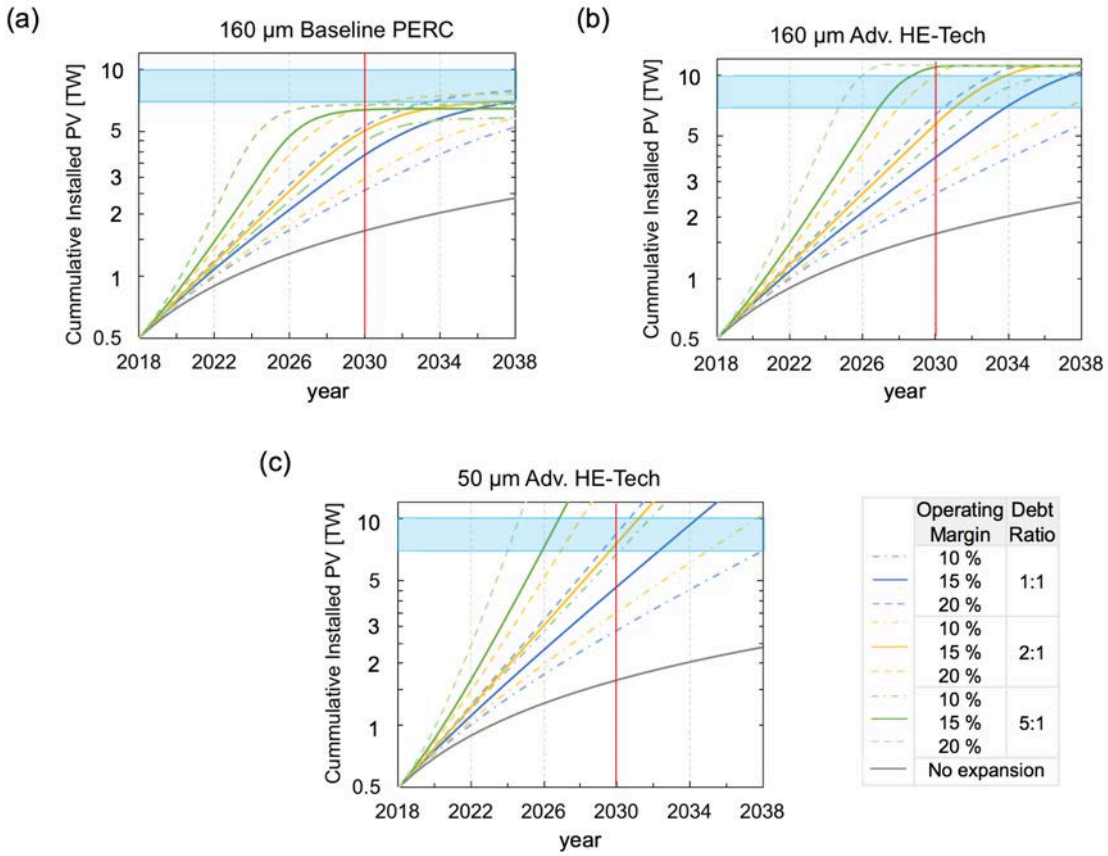

Figure S6: Cumulative PV installation over the next 20 years for adopting different technological concepts (using the growth model in Needleman et al. [3] with the updated cost values).

E. Operating margins for PV companies

The operating margins over the past five years for eight selected PV companies were calculated from the annual financial data of each company published on Yahoo Finance [4] (see Figure S7).

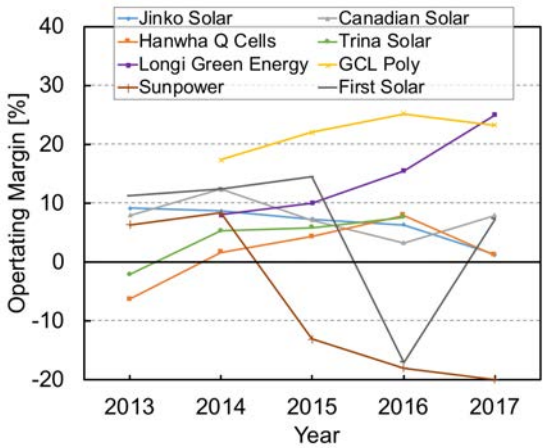

Figure S7: Operating margins of PV companies over the recent five years.

F. Waterfall Breakdown of the Capex and Cost Difference

The waterfall breakdown of the current PERC with 160 µm wafer to the HE-Tech with 50 µm wafer. Under the assumptions in our model, we find in Figure S8 that the efficiency scales down both cost and capex universally, while the silicon savings has slightly larger impact on capex reduction (~27%) than cost reduction (~14%). As the results of uncertainty analysis, the error bars indicate the capex or cost change in response to ±5% change of every specific factor. The error bar for the advanced HE-Tech module indicates the overall uncertainty range of capex or cost if all the variables are changed by ±5%.

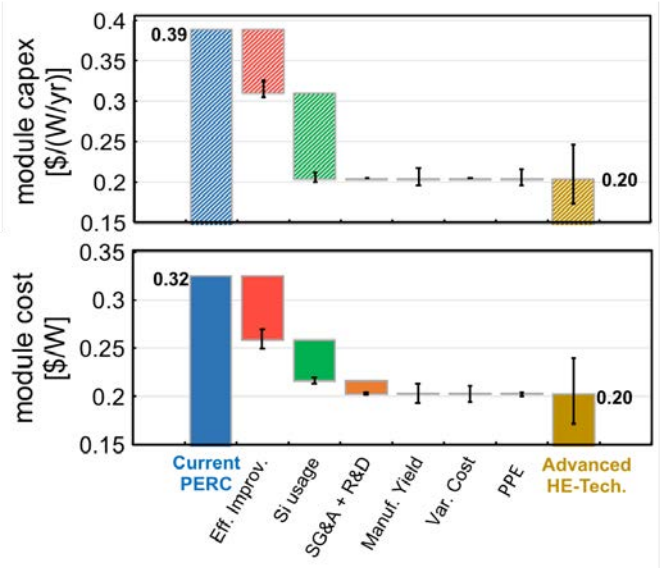

Figure S8: Waterfall chart of the capex and cost evolutions from the state-of-the-art PERC module with 19.0% efficiency and 160-µm-thickness wafer to the advanced concepts of advanced HE-Tech module with 23.8% efficiency and 50-µm-thickness wafer. The six factors in the breakdown are efficiency improvement, silicon saving, SG&A and R&D, manufacturing yield, direct variable cost and direct PPE. The bars with zero contributions indicate no change of the specific variable was considered in the cost model.

G. Silicon Kerf Loss vs Wafer Thickness

The amount of silicon kerf loss is limited by the wire sawing process. In the past decade, kerf loss by wire sawing process as shown in Figure S9 is steadily reduced from 200 to 95 µm [5]–[7], with the projected additional reduction down to 60 µm (ITRPV predicted technology limit of wire sawing [8]). As mentioned briefly, achieving kerf loss below 60 µm may require novel technology of kerfless wafer growth, *e.g.*, epitaxial lift-off or direct wafer growth. Particularly, for wafers with 50 µm thickness and 28 µm kerf loss will necessarily require those kerfless technologies.

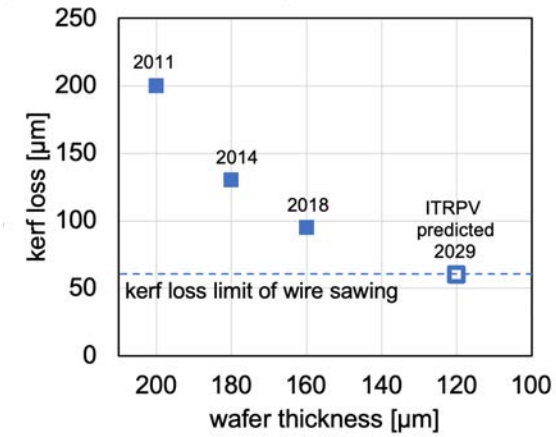

Figure S9: Silicon kerf loss vs wafer thickness for the past years from Ref. [5]–[7], and the ITRPV predicted kerf loss limit for wire sawing [8].

[1] N. M. Haegel, R. Margolis, T. Buonassisi, D. Feldman, A. Froitzheim, R. Garabedian, M. Green, S. Glunz, H.-M. Henning, B. Holder, I. Kaizuka, B. Kroposki, K. Matsubara, S. Niki, K. Sakurai, R. A. Schindler, W. Tumas, E. R. Weber, G. Wilson, M. Woodhouse, and S. Kurtz, "Terawatt-scale photovoltaics: Trajectories and challenges.," *Science*, vol. 356, no. 6334, pp. 141–143, Apr. 2017.

[2] "World Energy Outlook Special Report 2015: Energy and Climate Change," International Energy Agency, 2015.

[3] D. B. Needleman, J. R. Poindexter, R. C. Kurchin, I. M. Peters, G. Wilson, and T. Buonassisi, "Economically Sustainable Scaling of Photovoltaics to Meet Climate Targets," *Energy & Environmental Science*, vol. 9, pp. 2122–2129, 2016.

[4] "Yahoo Finance." [Online]. Available: finance.yahoo.com. [Accessed: 12-Oct-2018].

[5] D. M. Powell, M. T. Winkler, H. J. Choi, C. B. Simmons, D. B. Needleman, and T. Buonassisi, "Crystalline silicon photovoltaics: a cost analysis framework for determining technology pathways to reach baseload electricity costs," *Energy & Environmental Science*, vol. 5, no. 3, pp. 5874–5883, Mar. 2012.

[6] D. M. Powell, R. Fu, K. Horowitz, P. A. Basore, M. Woodhouse, and T. Buonassisi, "The capital intensity of photovoltaics manufacturing: barrier to scale and opportunity for innovation," *Energy & Environmental Science*, vol. 8, no. 12, pp. 3395--3408, 2015.

[7] M. Woodhouse, B. Smith, A. Ramdas, and Robert Margolis, "Crystalline Silicon Photovoltaic Module Manufacturing Costs and Sustainable Pricing: 1H 2018 Benchmark and Cost Reduction Roadmap," Golden, CO, USA: National Renewable Energy Laboratory (NREL), 2019.

[8] "International Technology Roadmap for Photovoltaics (ITRPV) Ninth Edition," 2018.