Electronic Supplementary Material (ESI) for Materials Horizons.

Supporting Information

A Meso-robotic Metamaterial that Uses Actuators and Sensors to Control its Properties

Chenyang Luo, Yuanping Song, Chang Zhao, Sridharan Thirumalai, Ian Ladner, Michael A. Cullinan, Jonathan B. Hopkins*

The information provided in each section of this document supports the corresponding content introduced and referenced in the main body of the paper.

A. Metamaterial actuator fabrication details

This section summarizes the 13 microfabrication steps (Fig. S1) used to make the actuators shown photographed in Fig. 3. The fabrication steps are:

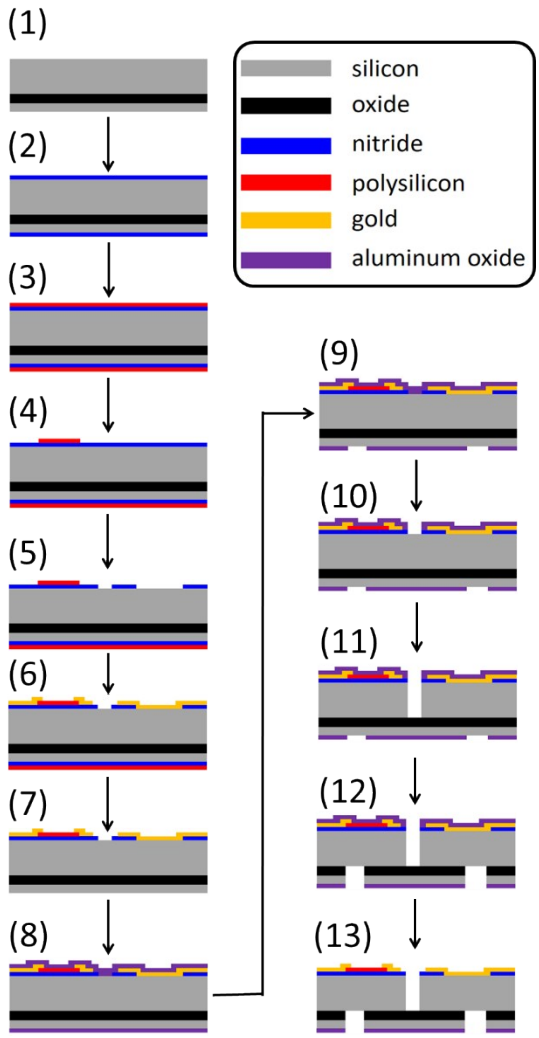

Figure S1. Microfabrication steps used to fabricate the actuators photographed in Fig. 3. The color-coding convention of this figure is consistent with the colors used to define the design in Fig. 1.

1) Start with a silicon-on-insulator (SOI) wafer with a 400 µm device layer, a 4 µm buried oxide (BOX) layer and a 50 µm handle layer.
2) Grow 200 nm of silicon nitride using a low pressure chemical vapor deposition (LPCVD) furnace
3) Grow 200 nm of amorphous silicon using LPCVD followed by a quick hydrofluoric acid (HF) dip to remove the native oxide layer. The amorphous silicon is then diffusion doped using a phosphoryl chloride gas at 900 °C for 20 minutes. The wafer is then annealed at 1050 °C for 30 minutes to drive in the dopant and to convert the amorphous silicon to polycrystalline silicon. Finally, a buffered oxide etch is used to clean the phosphosilicate glass layer that is formed during the diffusion process.
4) Define the piezoresistive strain gauge geometry using photolithography and then use reactive ion etching (RIE) (Plasmatherm 790RIE plasma etch) to transfer this pattern into the polysilicon layer.
5) Use photolithography to define and RIE to etch holes in the topside silicon nitride layer to be able to make electrical connections to the device layer.
6) Use photolithography to define a lift-off pattern of the electrical traces and bond pads. Then use e-beam evaporation (CHA Industries SE-1000-RAP) to deposit a 30 nm thick titanium adhesion layer followed by a 200 nm gold electrical trace layer followed by a liftoff process to remove the excess metal from the wafer.
7) Spin on photoresist on the top of the wafer to protect it during backside processing followed by an etch (Plasmatherm 790RIE plasma etch) of the backside polysilicon and silicon nitride layers. Remove the topside protective photoresist using an acetone etch.
8) Deposit 200 nm of aluminum oxide using atomic layer deposition (ALD, Cambridge NanoTech SavannahTM 200) on both sides of the wafer. The aluminum oxide is used as a hard mask for the deep silicon etching steps.
9) Preform photolithography on the backside pattern and use RIE (Oxford ICP RIE100) to etch the pattern in to the backside aluminum oxide hard mask layer.
10) Preform photolithography on the topside pattern and use RIE (Oxford ICP RIE100) to etch the pattern in to the topside aluminum oxide hard mask layer.
11) Use deep reactive ion etching (DRIE) (Nordson March px-250) to transfer the topside pattern into the device layer to define thermal actuators and flexures.
12) Use DRIE (Nordson March px-250) to transfer the backside

pattern into the device layer and use RIE (Oxford 80 RIE) to etch the silicon oxide BOX layer to release the device.

13) Etch (Oxford ICP RIE 100) the top side aluminum oxide hard mask to remove the protective mask and expose the electrical traces and bond pads.

B. Parameter sweep details

This section summarizes the details underlying the parameter sweep used to generate the plots of Fig. 2. The 11 independent parameters that were swept to optimize the actuator's geometry are described in Table S1 and labeled in Fig. S2a. Other less important parameters, which are also necessary to define the design's geometry, were fixed with the constant values shown in Fig. S2b. Note that the parameter labeled *W* in Fig. S2b is a function of the other 11 independent parameters (i.e., *W* is a dependent parameter). Whenever the parameter labeled *D* in Fig. S2c was less than 700 µm during the parameter sweep, the actuator geometry would belong within a special case labeled Case 1 in Fig. S2c and the parameter labeled *t* in Fig. S2b was set to 100 µm. Whenever *D* was greater than 700 µm, the actuator geometry would belong within a special case labeled Case 2 in Fig. S2c and the parameter labeled *t* in Fig. S2b was not applicable. As the 11 parameters were swept, the lengths labeled in Fig. S2d were constrained to be greater than the values shown so that the resulting geometry would be geometrically compatible and produce parts that would not collide during operation. The smallest and largest values that were set to bound each parameter's sweep are provided in Table S1. The smallest values were determined by the smallest feature sizes that could be fabricated and the largest values were selected to ensure that the full design space would be considered while recognizing that many designs within the sweep would be filtered out by the constraint conditions defined in Fig. S2d. The sweep resolution increments added to each parameter as they were swept from their smallest to their largest values are also provided in Table S1. The material properties used for each layer during the finite element analysis of each actuator design version in the parameter sweep are provided in Table S2. Note that the thermal expansion coefficient provided for silicon in this table is only true at room temperature. For the finite element analysis of this work, however, the thermal expansion coefficient of silicon was set to be a function of its temperature according to an empirical equation generated previously[1] because the design's thermal actuator beams are made of silicon and become hot when current is flown through their geometry.

C. Final device parameters

This section provides the final values selected for the 11 independent geometric parameters of the four devices shown in Figs. 2d and 3a. These values are given in Table S3.

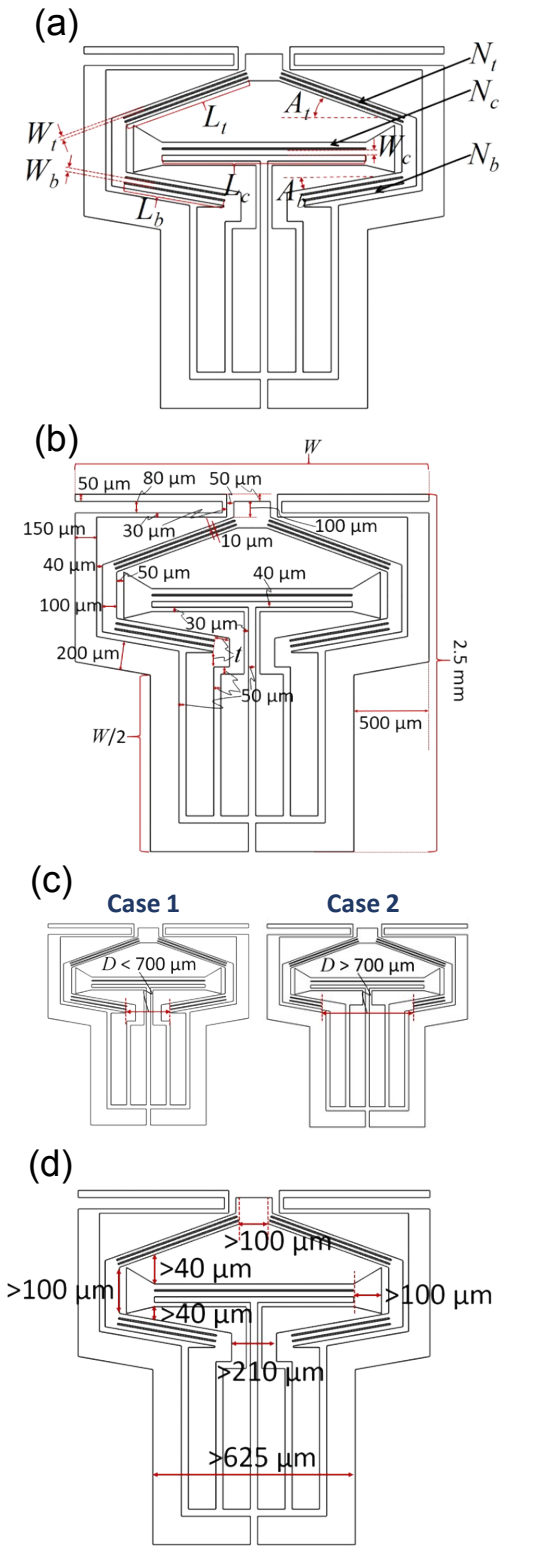

Figure S2. (a) Independent parameters that were swept to optimize the actuator's geometry; (b) other fixed parameters that define the remainder of the actuator's geometry; (c) two different geometry cases considered during the parameter sweep; (d) constraints used during the parameter sweep to ensure that features were able to be fabricated, were geometrically compatible, and would not collide during operation. Note that the drawings in this figure show only the outline of the device layer labeled "Silicon" in Fig. 1e.

Table S1. Detailed values used to sweep the 11 independent parameters.

Variable	Description	Smallest Value	Increment Size	Largest Value
N_c	Number of center beams	1	1	25
L_c	Length of center beams	0.1 mm	0.01 mm	2.5 mm
W_c	Width of one center beam	0.02 mm	0.01 mm	0.1 mm
A_b	Angle of bottom beams	1°	1°	45°
N_b	Number of bottom beams	1	1	25
L_b	Length of bottom beams	0.1 mm	0.01 mm	2.5 mm
W_b	Width of one bottom beam	0.02 mm	0.01 mm	0.1 mm
A_t	Angle of top beams	1°	1°	45°
N_t	Number of top beams	1	1	25
L_t	Length of top beams	0.1 mm	0.01 mm	2.5 mm
W_t	Width of one top beam	0.02 mm	0.01 mm	0.1 mm

Table S2. Material properties applied to the finite element analysis used to generate Fig. 2.

Constituent Material	Gold	Silicon Dioxide	Silicon
Density	19,300 kg/m^3	2,270 kg/m^3	2,330 kg/m^3
Thermal Expansion Coefficient	1.42x10^{-5} /C	5.00x10^{-7} /C	2.57x10^{-6} /C
Young's Modulus	79 GPa	70 GPa	166 GPa
Poisson's Ratio	0.44	0.17	0.28
Thermal Conductivity	31 W/(Cm)	1.4 W/(Cm)	148 W/(Cm)
Resistivity	2.19x10^{-8} Ωm	1.00x10^{17} Ωm	5.00x10^{-2} Ωm
Tensile Yield Strength	Not needed	155 MPa	166 MPa
Compression Yield Strength	Not needed	1,500 MPa	3,200 MPa

Table S3. Final parameters determined for the four devices of Figs. 2d and 3a.

Parameter	Device 1	Device 2	Device 3	Device 4
N_c	3	5	5	5
L_c	0.64 mm	0.60 mm	1.00 mm	0.90 mm
W_c	0.10 mm	0.02 mm	0.02 mm	0.02 mm
A_b	45°	9°	29°	8°
N_b	5	3	4	1
L_b	1.03 mm	0.80 mm	0.80 mm	0.80 mm
W_b	0.02 mm	0.05 mm	0.03 mm	0.05 mm
A_t	44°	34°	3°	2°
N_t	6	3	4	3
L_t	0.10 mm	0.50 mm	1.00 mm	1.33 mm
W_t	0.02 mm	0.02 mm	0.02 mm	0.02 mm

D. Envisioned lattice assembly

This section discusses how large lattices of the design of this paper could be assembled with enough precision and speed to enable the production of metamaterials that achieve actively controlled properties for practical commercial applications.

For this paper, the lattices were assembled by hand use tweezers and a jig to hold the MEMS devices in place as they were assembled. The devices were then wire bonded using a gold wire bonder (West Bond wire bonder model 7476D-79). This method works well for low production volumes but it is slow and imprecise for the assembly of large lattices.

For large scale production, we envision moving to a robotic pick-and-place system with flip-chip connections to fully assemble the lattices at higher rates and with more precision. In large-scale production, we would start with an application specific integrated circuit (ASIC) similar to the one shown in Fig. 1c. These ASICs can be fabricated at the size required for the design of this paper using standard CMOS processes at a commercial fab. However, ASIC design and fabrication is very expensive for low volume production, which is why the ASICs were not fabricated for this paper. Fortunately, the average cost of producing an ASIC goes down substantially as the volume of production goes up, so for large-scale lattice production, ASICs are expected to be cost effective.

Once the ASICs are fabricated, the MEMS chips will be assembled onto them using a flip-chip assembly process to form the metamaterial cells. In this process, solder bumps will be deposited onto the bond pads on the MEMS devices during the final wafer processing step. The MEMS device will then be flipped over so that the bond pads on the MEMS device face

the ASIC and a robotic pick-and-place tool will be used to align the bond pads on the MEMS device with the bond pads on the ASIC. Modern robotic pick-and-place tools are able to place millimeter-scale chips with sub-5μm accuracy which should be a more than sufficient tolerance for the assembly of the metamaterial lattices. Once the MEMS devices have been placed on the ASIC, the assembly will be heated to allow the solder to reflow and complete the interconnect. The assembly will then be rotated using a custom designed jig and the process will be repeated until a full cell is assembled. Once enough cells are assembled in this way, a similar robotic assembly system would solder the cells together to form the lattice.

References

1 Y. Okada and Y. Tokumaru, *J. Appl. Phys.*, 1984, **56**, 314–320.