Electronic supporting Information

Asymmetric Hot Carrier Tunneling van der Waals Heterostructure for Multibit Optoelectronic Memory

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1. Ambient Stability of PtS_2 and the memory device after months.

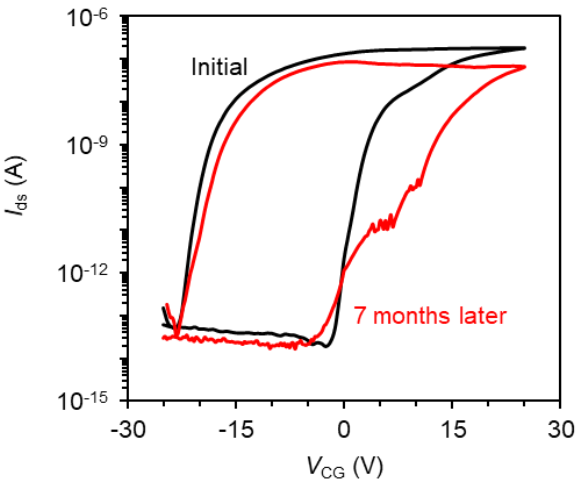

Fig. S1. The stability of electrically programmed hysteresis of memory after seven months, implying the excellent stability of PtS_2 in ambient environments.

2. Control experiments on thin PtS_2 flake

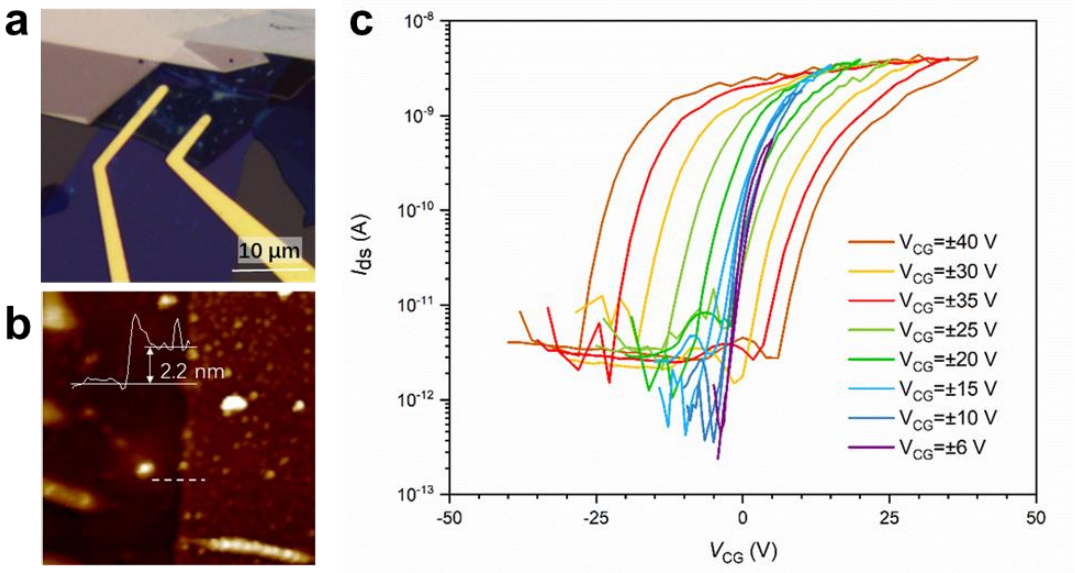

Fig. S2. Transfer curves of the float gate heterostructure using thin PtS_2 flake (2.2 nm) as the semiconductor channel, in which a ON/OFF ratio of 10^3 is obtained.

3. IV characteristic of the initial memory and at ON and OFF states.

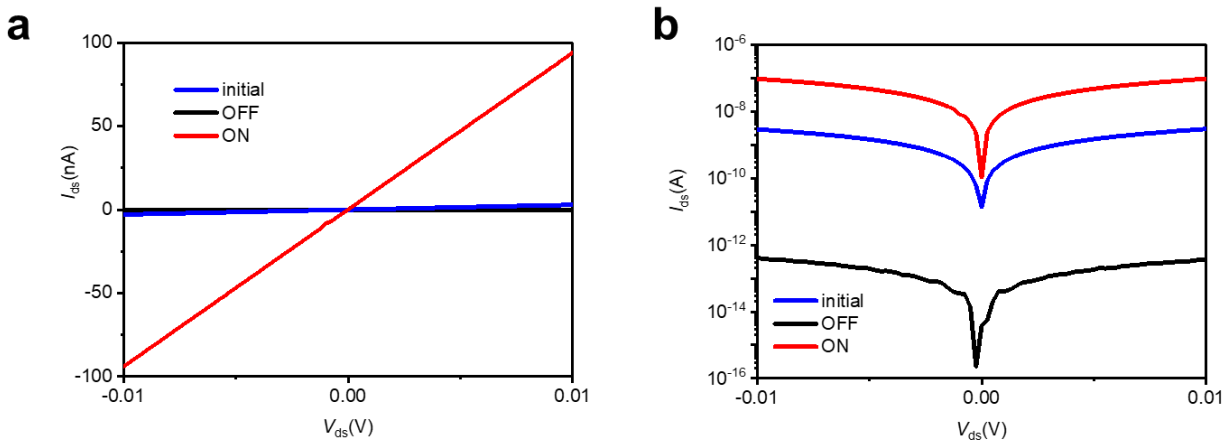

Fig. S3. IV characteristic of the initial memory and under ON and OFF states. The ohmic contact to PtS_2 is vital for the obtained large ON/OFF ratio in memory without Schottky contact limited ON states.

4. Extraction of threshold voltage for ON and OFF states of the memory.

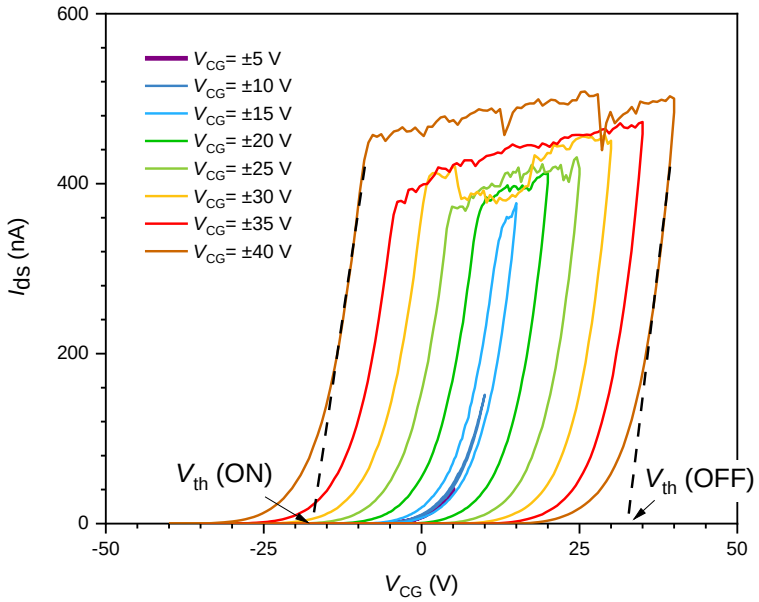

Fig. S4 The transfer curves of the float gate memory when sweeping V_{CG} in different ranges from ±5 to ±40 V. The threshold voltage (V_{th}) at ON and OFF states are extracted from the linear extrapolation of respectively the left and right side of the loop.

5. Retention and pulsed program/erase characteristic of the memory.

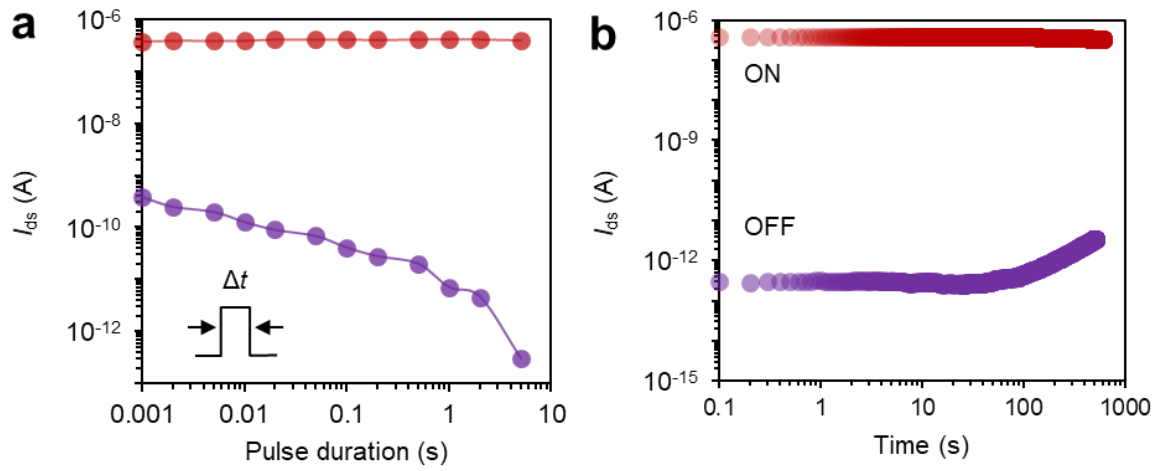

Fig. S5. a) Effect of the width of electric pulse (30 V) on the read current at ON and OFF states. b) The measured retention characteristic of memory. When reducing the duration of electric pulse, the trapped charges in float gate is reduced depends on the magnitude of tunneling current and the capacitance of float gate. As a result, short electric pulse tends to lead to lower ON/OFF ratio. It is also observed that the erase process shows more dependence on the electric pulse duration compared to the program. This is attributed to the higher charge tunneling barrier during erase than the program discussed in the manuscript.

6. Optical image of a device with and without graphene float gate.

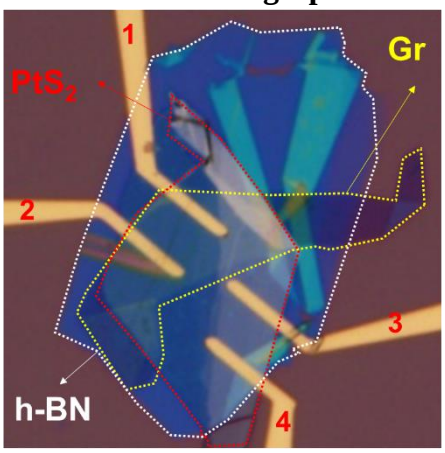

Fig. S6. Optical image of a control device having both PtS_2/h-BN/Gr and PtS_2/h-BN structure, from what the role of graphene float gate on memory performance is studied.

7. Transfer curves and retention characteristic of the device with and without graphene float gate.

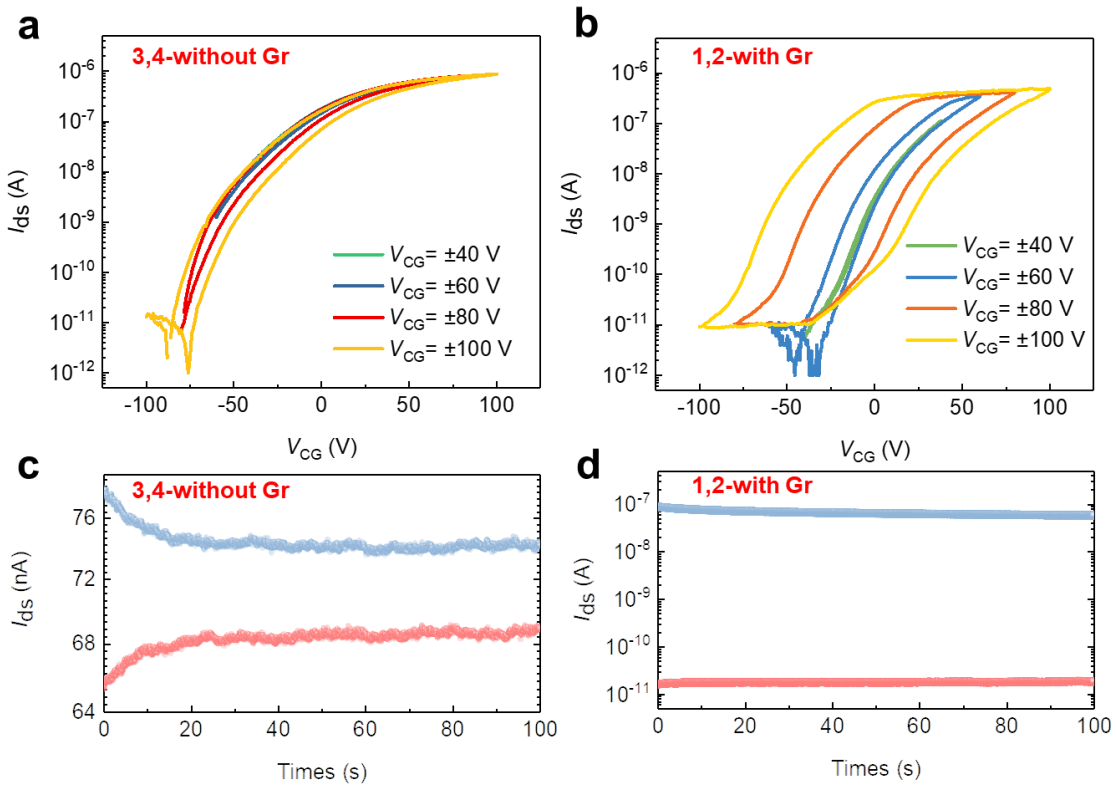

Fig. S7. Transfer curves and retention characteristic of the devices with or without graphene float gate: (a), (c) without float gate; (b), (d) with float gate.

8. 2D map of programmed/erased ON/OFF states via synchronized electric and light pulses.

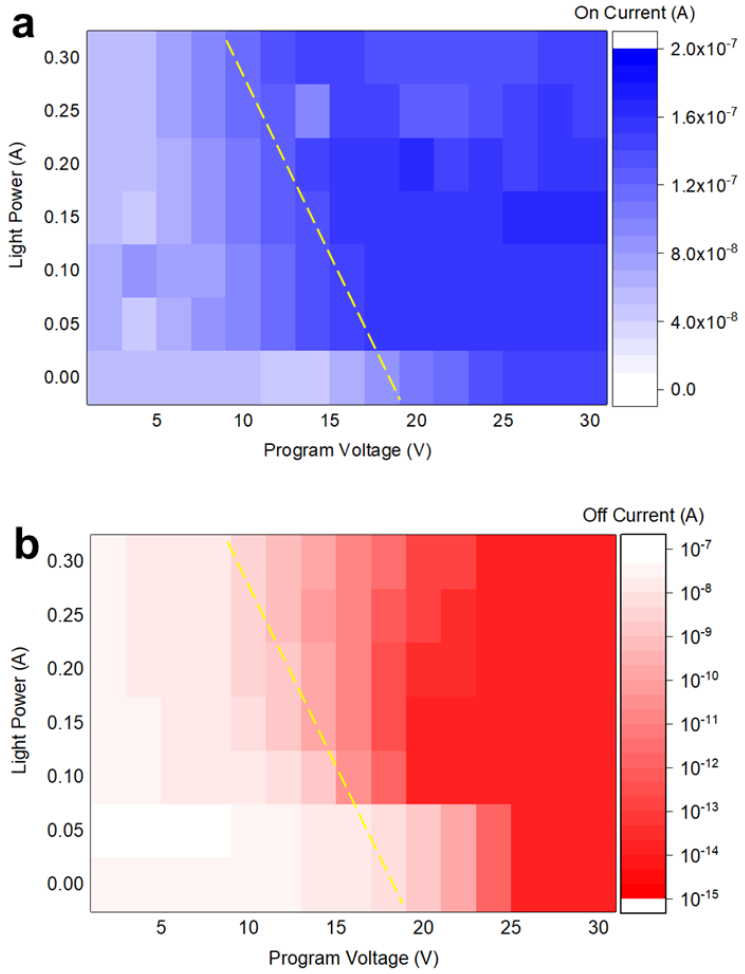

Fig. S8. 2D map of the ON and OFF state conductance programmed/erased by synchronized electric and light pulses.

9. Transient conductance change in memory by light exposure

To model the transient conductance change, the charge injection across h-BN by light exposure is modeled by numerically solving the coupled *Eq.* 1-3, using the effective tunneling barriers as the fit parameter.

$$\mathrm{J_t}(t) = \frac{A}{\Phi_B} E_{\mathrm{ox}}^2(t) \exp\left(-\frac{B\Phi_{\mathrm{B}}^{\frac{3}{2}}}{E_{\mathrm{ox}}(t)}\right) \quad (1)$$

$$\frac{dQ_{\mathrm{tr}}(t)}{dt} = -J_t\left(V_{\mathrm{FG}}, P_{\mathrm{light}}\right) \quad (2)$$

$$Q_{\mathrm{tr}}(t) = V_{\mathrm{FG}}(t) C_{\mathrm{FG}} \quad (3)$$

where A and B are constants, Φ_{B} is the effective barrier height and E_{ox} is the electric field throughout dielectric layer, S is the active device area and C_{FG} is the capacitance between float gate and PtS_2 channel.

To further fit the measurement results, the charge trapping Q_{tr} in h-BN need to be converted to observable conductance in experiments. This is achieved by firstly transform Q_{tr} into an equivalent V_{CG} that causes same potential drop across h-BN. The conductance in PtS_2 is then approximated based on the interpolation of a hysteresis corrected transfer (I~V_{CG}) curve in Fig. 1d. As illustrated in following Fig. S9, the transient conductance change of the memory in ON and OFF states by light exposure could be well described using the asymmetric tunneling barriers of 0.26 eV for hole tunneling from graphene to PtS_2 and 0.1 eV for the reverse tunneling.

10. Numerical fitting to the light induced transient conductance change by light exposure.

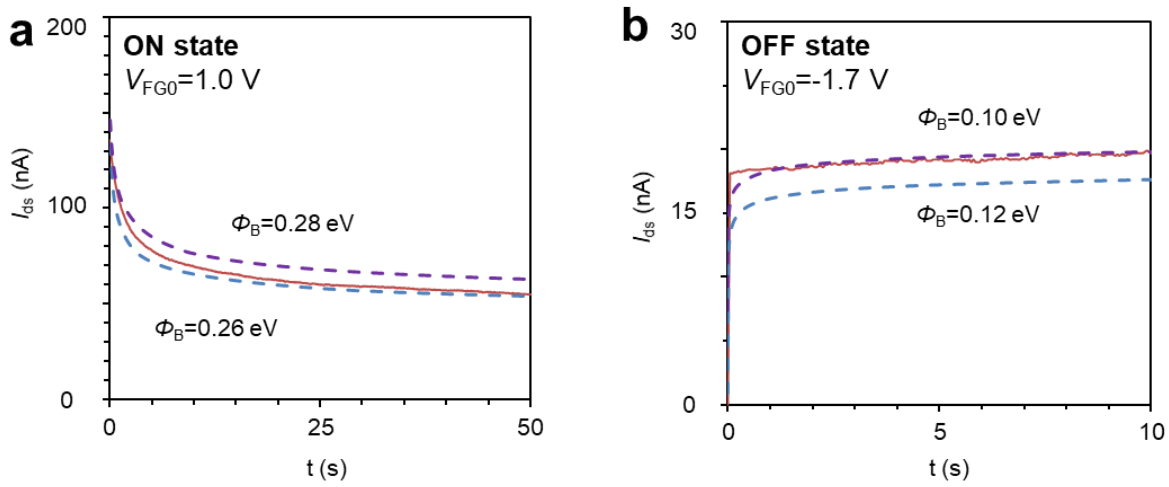

Fig. S9. Numerical fitting to the transient change of memory states in a) ON and b) OFF states by light exposure.

11. Optical program behavior of a float gate memory of MoS_2/h-BN/graphene.

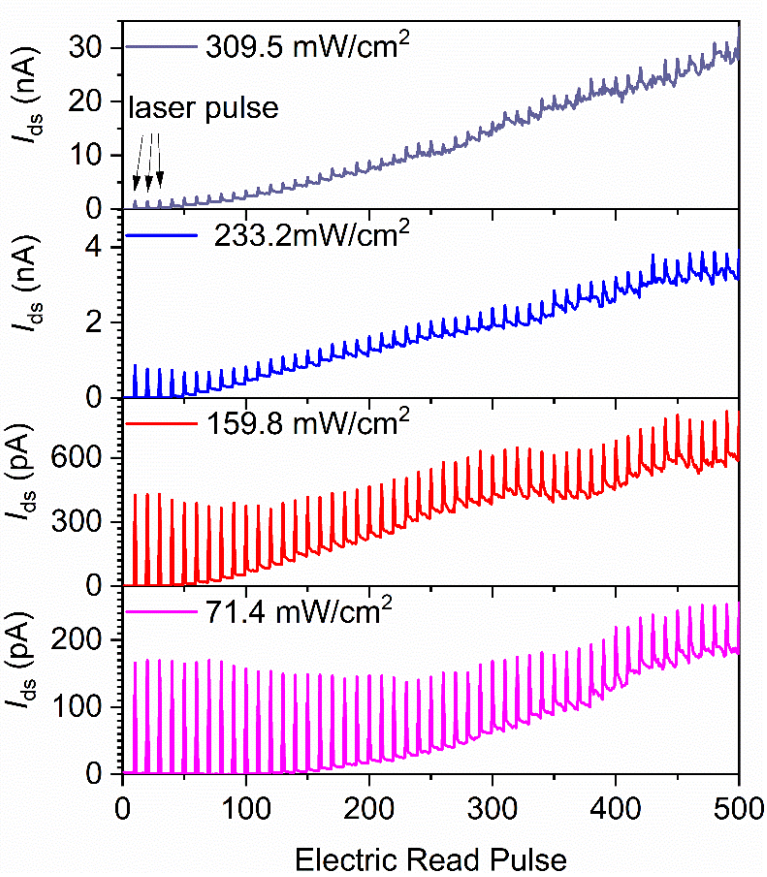

Fig. S10. Optical program behavior of a convention device fabricated by MoS_2/h-BN/graphene. The memory is first erased by an electric pulse of V_{CG}=25 V and then exposed to light pulses of different light intensity. The thickness of MoS_2 and h-BN is respectively 5.1 and 11.3 nm.

12. Effect of light intensity to the optical programmed conductance states in memory.

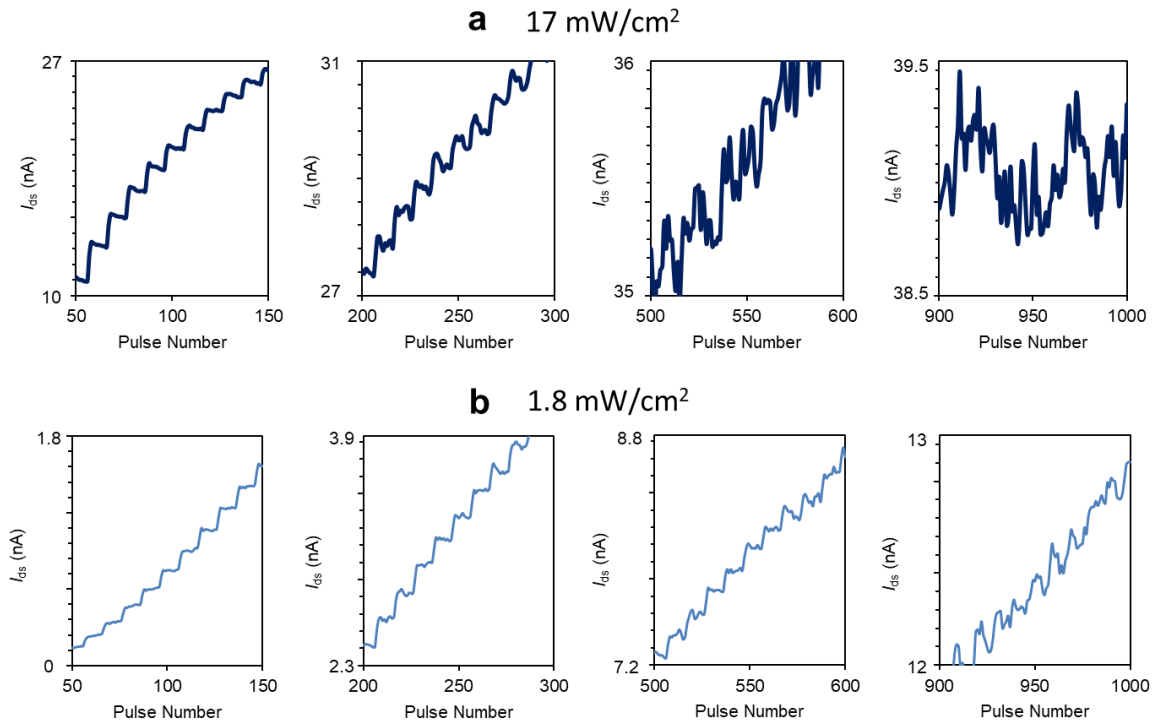

Fig. S11. The multibit memory states programmed via 532 nm light pulses at the intensity of 1.8 and 17 mW/cm^2. Light pulses of low intensity render more distinguishable memory states compared to high intensity pulses by avoiding rapid saturation of conductance states.

13. Multi-bit sates achieved with a convention device of MoS_2/h-BN/graphene.

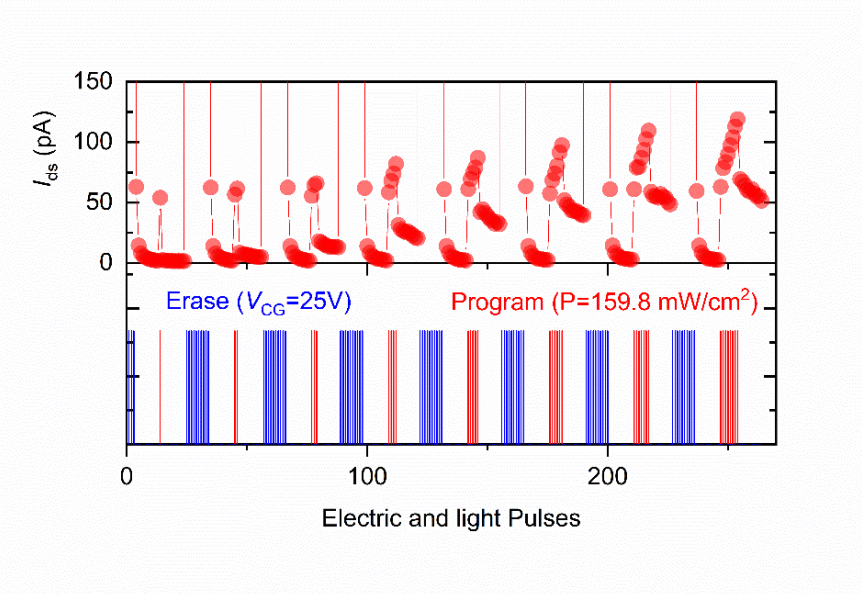

Fig. S12. Optical program behavior of a convention device fabricated by MoS_2/h-BN/graphene. The memory is first erased by an electric pulse of V_{CG}=25 V and then exposed to light pulses of different pulse number.