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High performance indium oxide nanoribbon FETs: Mitigating devices signal variation from batch fabrication

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1. Image reversal lithography process and sputtering conditions

The fabrication process utilizes 2 image reversal photolithography to define the patterns of In_2O_3 nanoribbon and metal contact lines. The process is carried out in the following steps and conditions: Step 1: the wafer was washed with acetone and isopropanol and then blew dry with N_2 gas and dried on a hotplate at 200^0C for 2 min and then the wafer is allowed to rest at room temperature for a few min to cool down. Step 2: The wafer was mounted onto a spin coater (Suss Delta 80). About 3 mL of positive photoresist AZ5214E was dispensed onto the wafer and spun at 4000 rpm. Step 3: the wafer is pre-baked at 100^0C in 1 min to evaporate the solvent in the photoresist. Step 4: The first exposure dose was applied using The EVG 620 Mask Aligner with a constant dose of 10 mJ/cm^2. The exposed wafer is image reversal baked on a hotplate at 115^0C in 1 min 20s. Step 5: The wafer is exposed a second time using constant dose of 120 mJ/cm^2 with a blank photomask. Deposition of In_2O_3 was conducted using radio frequency sputtering at 50 W in Ar plasma (Ar gas flow rate: 10.0 Sccm). Sputtering of Cr and Au was done using direct current sputtering

2. Device characterization

The field effect behaviour of the device was characterized in 1X PBS (pH 7.5, electrical conductivity = 15.5 mS/cm) within a customized Faraday box so that we could extract operational parameters for the device from characterization data.

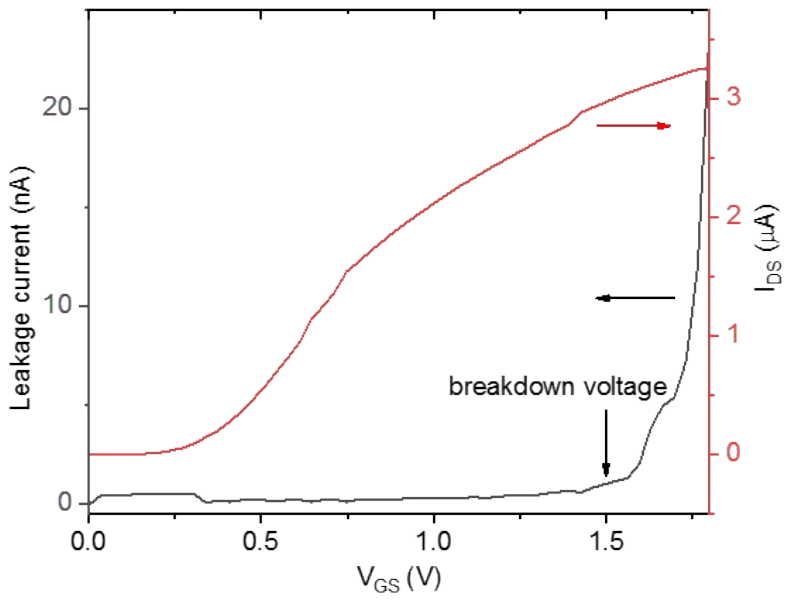

Fig. S1 Drain and leakage current of the fabricated representative In_2O_3 NR FET

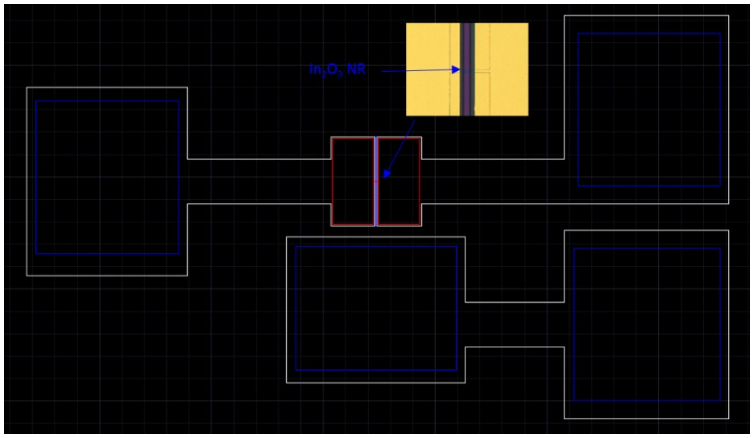

Fig. S2 Design of 1 In_2O_3 NR FET channel with on-chip integrated gate electrode. Areas within blue rectangles are opening areas to serve as gate electrode and bonding pads. The inset is confocal image of the centre of the chip showing the sensing area with In_2O_3 NR

3. Statistical analyses of electrical characteristics of the devices

Statistical analyses of the threshold voltage, maximum transconductance, field-effect mobility, and drain current on/off ratios for the In_2O_3 NR FET devices are presented in Fig. S3 below:

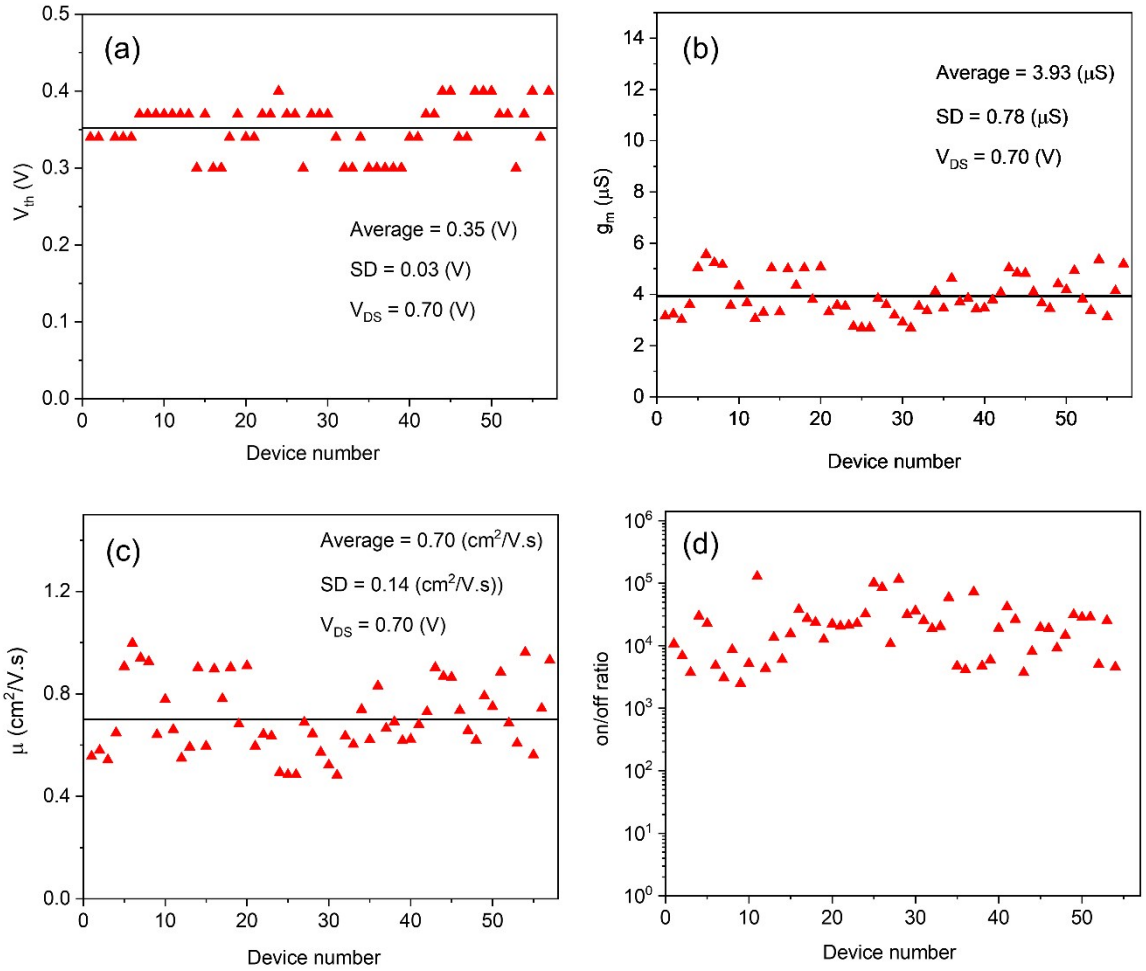

Fig. S3 Plots of electrical characteristics for the 57 tested In_2O_3 NR FETs: (a) Threshold voltage, V_{th}; (b) Transconductance, g_m; (c) Field effect mobility, μ; (c) Drain current on/off ratio.

4. Signal normalization

Small variations of device-to-device always exist in microfabrication. Hence, it is a common practice to normalize the drain currents evaluation of the device performance and sensing applications. [3-6] Signal normalization is usually carried out by taking the ratio of I/I_0, where I_0 is the I_{DS} response of the FET at the V_{GS0} and I is the Ids response of the FET at different V_{GS}. In this work, I_0 is selected at the lowest possible V_{GS} applied in the respective regime (e.g. V_{GS} = 0.17 V for subthreshold and V_{GS} = 0.51 V for linear) assuming in the actual sensing the device is biased at these initial gate voltage points. Data point distributions of the two operation regimes when normalized against the highest I_{DS} are provided in Fig. S4 below.

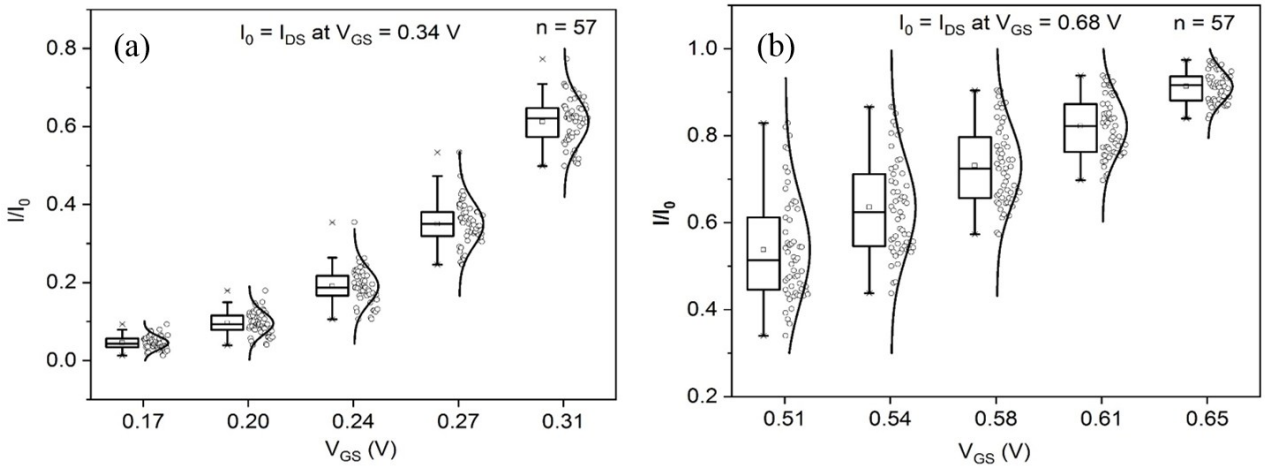

Fig. S4 (a) Distributions of normalized drain currents in the subthreshold (a) and linear (b) regimes when normalized against the highest I_{DS} in the respective regimes ($I_0 = I_{DS}$ at V_{GS} = 0.34 V in subthreshold; $I_0 = I_{DS}$ at V_{GS} = 0.68 V in linear)

5. Signal resolution

Graphs of I/I_0 versus applied V_{GS} in the subthreshold and linear regimes:

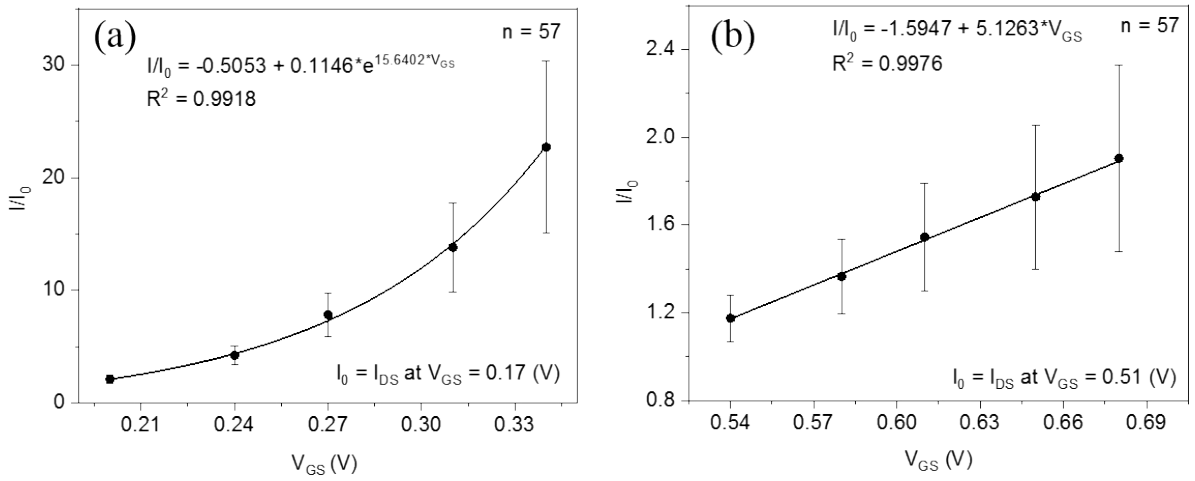

Fig. S5 I/I_0 responses against different applied V_{GS} in the subthreshold regime (a), and in the linear regime (b); Error bars are SD of 57 devices.

6. References

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