Electronic Supplementary Material (ESI) for Nanoscale Advances.
This journal is © The Royal Society of Chemistry 2020

Electronic supplementary information

Does carrier velocity saturation help to enhance f_{max} in graphene field-effect transistors?

Pedro C. Feijoo[1], Francisco Pasadas[1], Marlene Bonmann[2], Muhammad Asad[2], Xinxin Yang[2], Andrey Generalov[3], Andrei Vorobiev[2], Luca Banszerus[4], Christoph Stampfer[4], Martin Otto[5], Daniel Neumaier[5], Jan Stake[2], David Jiménez[1]

[1] Universitat Autònoma de Barcelona, 08193 Cerdanyola del Vallès, Spain
[2] Chalmers University of Technology, SE-41296 Gothenburg, Sweden
[3] Aalto University, FI-00076 Helsinki, Finland
[4] 2nd Institute of Physics, RWTH Aachen University, 52074 Aachen, Germany
[5] Advanced Microelectronic Center Aachen, AMO GmbH, 52074 Aachen, Germany

S1. Fabrication and characterization of GFETs

The two-finger gate GFET analyzed in this work was fabricated as described in ref. 1. The reported state-of-the-art RF performance is achieved by a combination of improvements of the GFET design and fabrication process. First, a very high-quality CVD graphene film, with a Hall mobility up to 7000 $cm^2\,V^{-1}\,s^{-1}$, was transferred to a high-resistivity Si/SiO_2 substrate with an increased SiO_2 thickness of 1 μm, which resulted in a reduction in the parasitic pad capacitances. Immediately after the transfer, the graphene film was covered by a 5 nm thick protective Al_2O_3 layer. The protective layer encapsulates graphene and prevents it from contamination during further processing, thereby reducing concentration of traps and charged scattering impurities at the graphene/dielectric interface. Apparently, the use of a buffered oxide etching for opening contact windows in the protective Al_2O_3 layer resulted in a more effective removal of e-beam resist and PMMA residues and, hence, an extremely low graphene/metal specific contact resistivity, as low as 90 Ω μm.

The DC current-voltage curves and the scattering parameters S of the GFETs were measured using a Keithley 2612B dual-channel source meter and an Agilent N5230A network analyzer, respectively. The RF measurement setup was calibrated at the ground-source-ground microwave probe tips using a CS-5 calibration substrate by the SOLT procedure. The output characteristics (I_{ds}-V_{ds}) were obtained during the S-parameter measurements with a holding time of 30 s at each bias point. This holding time is long enough for the trapping/detrapping processes to stabilize. The S-parameters were measured under different bias conditions in the frequency range of 1–50GHz and used to calculate the admittance parameters Y, the small-signal current gain (h_{21}) and the unilateral power gain (U).[2–4] The equations used are included in section S5. The

experimental values of $f_{T,x}$ and f_{max} were found as the frequencies at which the extrapolation of the magnitudes of $|h_{21}|$ and $|U|$ equals to 0 dB.

S2. Self-consistent simulator including self-heating effect

Here we explain the fundamentals of the self-consistent simulator used to calculate the behavior of GFETs with a structure as depicted in Fig. 1(b) of the main text. More details of the simulator can be found thoroughly described in ref. 5. The intrinsic bias voltages applied to the electrodes of top gate and drain with respect to the source (V'_{gs} and V'_{ds}, respectively) induce a sheet charge density $\sigma(y) = q[p(y) - n(y)] + \sigma_{it}(y)$ in the graphene layer. The magnitudes $p(y)$ and $n(y)$ are the hole and electron concentrations along the graphene channel, q is the elementary charge, y is the axis that goes from source ($y = 0$) to drain ($y = L_g$), where L_g is the channel length. Here $\sigma_{it}(y)$ corresponds to the interface trapped charge density. The sheet charge distribution is needed to calculate the electrostatic potential $\psi(x,y)$ inside the GFET by means of the Poisson's equation. Fig. S1 shows the two-dimensional domain where this equation is solved, where x is the position along the axis that goes from back to top gate electrodes. Assuming that the GFET width W_g (in the z direction) is large as compared with the other dimensions of the device, the Poisson's equation can be written as follows:

$$\nabla \cdot [\varepsilon_r(x,y)\varepsilon_0 \nabla \psi(x,y)] = \rho_{free}(x,y) \quad \text{(S1)}$$

where ε_0 is the vacuum dielectric constant, and $\varepsilon_r(x,y)$ is the relative dielectric constant, which is equal to ε_t and ε_b inside the top and back dielectrics, respectively, and ε_G in the graphene. From Fig. S1, the parameters t_t and t_b correspond to the top and back insulator thicknesses, respectively. The charge density $\rho_{free}(x,y)$ is zero inside both dielectrics so its only contribution corresponds to $\sigma(y)$ inside graphene. When solving the Poisson's equation, the electrostatic potential on the top gate is set to $V'_{gs} - V_{gs0}$ and the back gate to $V'_{bs} - V_{bs0}$, where V_{gs0} and V_{bs0} are the flatband voltages. Homogeneous Neumann's conditions are applied to the other two boundaries of the dielectrics to ensure charge neutrality.

The drift-diffusion equation for the drain current I_{ds} reads as follows:

$$I_{ds} = qW_g[n(y) + p(y)]\mu(y)\frac{dV(y)}{dy} \quad \text{(S2)}$$

where $\mu(y)$ is the field-dependent mobility, assumed to be equal for electrons and holes, and $V(y)$ is the quasi-Fermi potential in the graphene. The boundary conditions make $V(y)$ equal to zero at $y = 0$ and equal to V'_{ds} at $y = L_g$. Electron and holes share the same quasi-Fermi level due to a very short recombination time of carriers in graphene, of around 10 - 100 ns.[6,7]

In this work we have included the effect of self-heating when calculating charges and current at a certain DC bias. This means that the temperature of the GFET rises due to the heat dissipated by the current flow along the graphene channel and is not properly

removed from the device because of the thermal resistance of the surrounding layers. We thus solve self-consistently the previous two-equation system (drift-diffusion and Poisson's equations) together with the solution of the equivalent thermal circuit of Fig. S2(a). The temperature of the graphene channel T must increase as:

$$T - T_0 = R_{\text{th}} P_{\text{dis}} \tag{S3}$$

where T_0 = 300 K is the temperature of the heat sink, assumed to be the environment of the transistor, and P_{dis} is the dissipated power in the GFET. In this work, the value of thermal resistance R_{th} has been considered as a fitting parameter to reproduce the experimental current-voltage curves. P_{dis} takes the form:

$$P_{\text{dis}} = |I_{\text{ds}} V'_{\text{ds}}| \tag{S4}$$

From both the electrostatic and quasi-Fermi potentials, the carrier concentrations are calculated using the linear dispersion relation of graphene, and thus accounting for its quantum capacitance:

$$n(y) = \rho_0 + N_{\text{G}} \mathcal{F}_1 \left[q \frac{\psi(0,y) - V(y)}{kT} \right] \tag{S5a}$$

$$p(y) = \rho_0 + N_{\text{G}} \mathcal{F}_1 \left[-q \frac{\psi(0,y) - V(y)}{kT} \right] \tag{S5b}$$

$$\sigma_{\text{it}}(y) = -q^2 N_{\text{it}} [\psi(0,y) - V(y)] \tag{S5c}$$

We have added the contribution of graphene puddles ρ_0 to the carrier concentrations.[8] Here, k is the Boltzmann constant, T is the temperature, N_{it} is the density of defects, which is assumed to be constant, and N_{G} is the effective density of states of graphene, given by:

$$N_{\text{G}} = \frac{2}{\pi} \left(\frac{kT}{\hbar v_{\text{F}}} \right)^2 \tag{S6}$$

being $\hbar$ the reduced Planck's constant and v_{F} the Fermi velocity (10^8 cm s^{-1}). In equation (S5), $F_1(z)$ refers to the first order Fermi-Dirac integral:

$$\mathcal{F}_i(z) = \frac{1}{\Gamma(i+1)} \int_0^\infty \frac{u^i \mathrm{d}u}{1 + e^{u-z}} \tag{S7}$$

The field-dependent mobility model that we have used in this work includes velocity saturation effects in the following form:

$$\mu(y) = \frac{\mu_{\text{LF}}}{\left\{ 1 + \left[\frac{\mu_{\text{LF}}}{v_{\text{sat}}(y)} \left| \frac{\partial \psi(0,y)}{\partial y} \right| \right]^\gamma \right\}^{\frac{1}{\gamma}}} \tag{S8}$$

where γ is a parameter of the model describing the softness of the crossover between low-field and high-field mobilities, and μ_{LF} refers to the low-field carrier mobility.

Saturation velocity v_{sat} is related to optical phonon emission energy $\hbar\Omega$, the carrier concentration $\rho_{\text{sh}}(y) = n(y) + p(y)$ and T by the following equation:

$$v_{\text{sat}}(y) = \frac{2\Omega}{\pi \sqrt{\pi \rho_{\text{sh}}(y)}} \sqrt{1 - \frac{\Omega^2}{4\pi v_{\text{F}}^2 \rho_{\text{sh}}(y)}} \frac{1}{N_{\text{OP}} + 1} \tag{S9}$$

Phonon occupation N_{OP} depends on temperature as:

$$N_{\mathrm{OP}} = \frac{1}{e^{\frac{\hbar\Omega}{kT}} - 1} \tag{S10}$$

In summary, given the set of material properties and the dimensions of the GFET, and after selecting a bias point (V'_{gs} and V'_{ds}), the simulator solves in a self-consistent way the drift-diffusion transport equation (S2) coupled with the 2D Poisson's equation (S1) together with self-heating equation (S3). The simulator then obtains the stationary values of I_{ds}, T, $n(y)$, $p(y)$, $\psi(x,y)$ and $V(y)$ as the outputs. In this work, we have used the values presented in Table S1 for the material properties and dimensions of the GFET, which correspond to the fabricated GFET described in the main text.

The extrinsic voltages V_{gs} and V_{ds} , connected to the terminals of the GFET, are related to the intrinsic voltages at the active area of the device by the following equations:

$$V_{\mathrm{gs}} = V'_{\mathrm{gs}} + R_{\mathrm{s}} I_{\mathrm{ds}} \tag{S11a}$$

$$V_{\mathrm{ds}} = V'_{\mathrm{ds}} + (R_{\mathrm{d}} + R_{\mathrm{s}}) I_{\mathrm{ds}} \tag{S11b}$$

where $R_{\mathrm{s}} = R_{\mathrm{d}} = R_{\mathrm{c}}/2$ are the series resistances at source and drain, which account for the metal-graphene contact resistance together with the access resistance due to the ungated graphene channel.

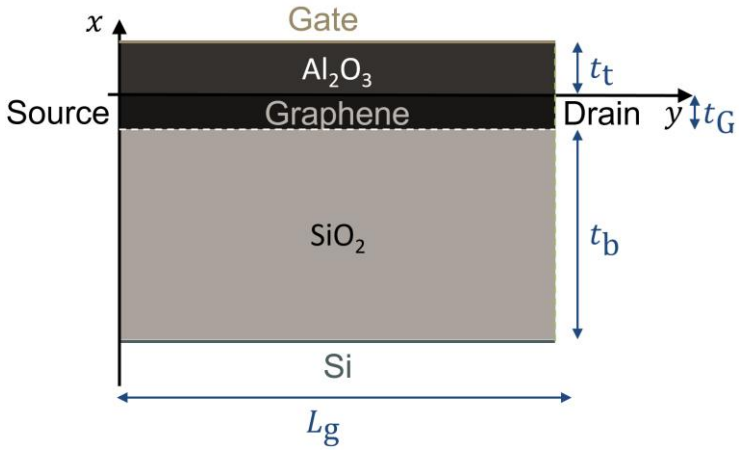

Fig. S1 Cross section of the GFET along channel length and the domain where the Poisson's equation is evaluated. This GFET active area corresponds to the dashed rectangle in Fig. 1(b) of the main text.

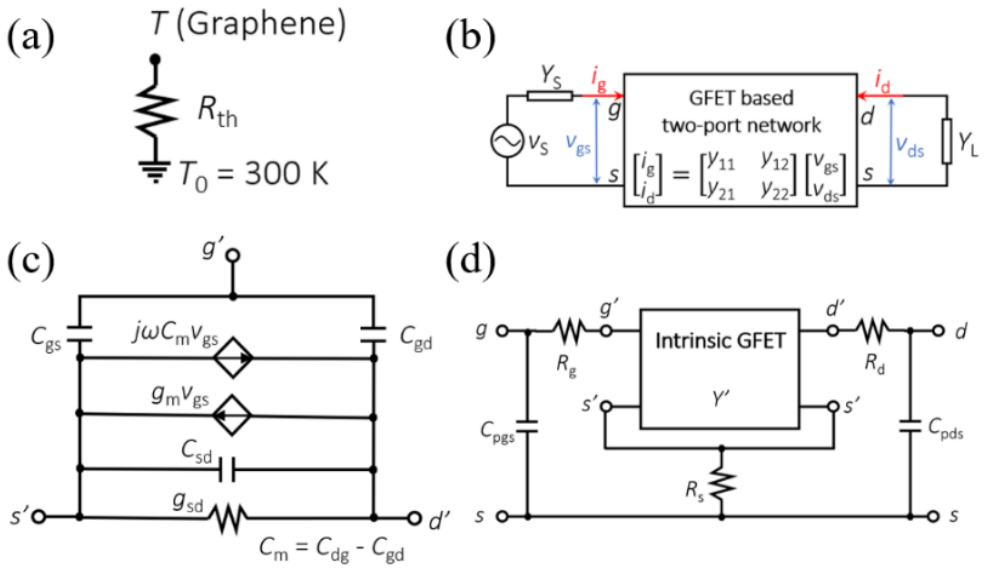

Fig. S2 (a) Thermal model assumed for the GFET. (b) GFET configured as a two-port network, with the input port formed by the gate-source terminals and the output port by the drain-source terminals. (c) Intrinsic equivalent circuit of the GFET. (d) Extrinsic embedding network with the parasitic series resistances, R_g, R_d, and R_s and the parasitic capacitances between gate and source (C_{pgs}) and between drain and source (C_{pds}).

Table S1 Parameters of the simulated GFET.

Parameter	**Value**
t_t	22 nm
t_b	1 µm
ε_t	7.5
ε_b	3.9
ε_G	3.3
L_g	500 nm
W_g	2×15 µm

S3. Definition of diffusion velocity and total velocity

In the drift-diffusion current given by Eq. (S2), we can define the total carrier velocity, v_{tot}, as the ratio between I_{ds} and the total carrier concentration, so:

$$v_{\mathrm{tot}}(y) \equiv -\frac{I_{\mathrm{ds}}}{q[n(y)+p(y)]} = -\mu(y)\frac{\mathrm{d}V(y)}{\mathrm{d}y} \tag{S12}$$

We can now separate the current into its drift and diffusion contributions. Particularly, the drift current can be expressed in terms of the drift velocity, v_{drift}, which is proportional to the electric field $\xi(y)$ which, in turn, can be written in terms of the (negative) gradient of the electrostatic potential $\psi(y)$:

$$v_{\mathrm{drift}}(y) = \mu(y)\xi(y) = -\mu(y)\frac{\mathrm{d}\psi(0,y)}{\mathrm{d}y} \tag{S13}$$

Now we can define a diffusion velocity, v_{diff}, related with the diffusion mechanism transport, as the difference between v_{tot} and v_{drift}.

$$v_{\mathrm{diff}}(y) = v_{\mathrm{tot}}(y) - v_{\mathrm{drift}}(y) = \mu(y)\frac{\mathrm{d}}{\mathrm{d}y}[\psi(0,y) - V(y)] \tag{S14}$$

where $\psi(0,y)$ – $V(y)$ corresponds to the local chemical potential. Figure S2 presents the microscopic distribution along the channel of the most important parameters simulated with our model, that is, $n(y)$, $p(y)$, $\psi(0,y)$, $V(y)$, $\psi'(0,y)$, $V'(y)$, $\mu(y)$, $v_{\mathrm{drift}}(y)$, $v_{\mathrm{diff}}(y)$ and $v_{\mathrm{sat}}(y)$, for the GFET simulated in this work and at a bias where f_{max} is maximum.

Since carrier velocities v_{tot}, v_{drift} and v_{diff} , together with v_{sat}, are magnitudes that are defined locally inside the graphene, we can average their values along the channel length in order to study their average behavior as a function of the bias. The averaged values are given by the following formulas, and have been represented in Fig. 6(f) and (g) in the main text.

$$\langle v_{\mathrm{drift}}\rangle = \frac{1}{L_{\mathrm{g}}}\int_0^{L_{\mathrm{g}}} v_{\mathrm{drift}}(y)\mathrm{d}y \tag{S15a}$$

$$\langle v_{\mathrm{diff}}\rangle = \frac{1}{L_{\mathrm{g}}}\int_0^{L_{\mathrm{g}}} v_{\mathrm{diff}}(y)\mathrm{d}y \tag{S15b}$$

$$\langle v_{\mathrm{tot}}\rangle = \frac{1}{L_{\mathrm{g}}}\int_0^{L_{\mathrm{g}}} v_{\mathrm{tot}}(y)\mathrm{d}y \tag{S15c}$$

$$\langle v_{\mathrm{sat}}\rangle = \frac{1}{L_{\mathrm{g}}}\int_0^{L_{\mathrm{g}}} v_{\mathrm{sat}}(y)\mathrm{d}y \tag{S15d}$$

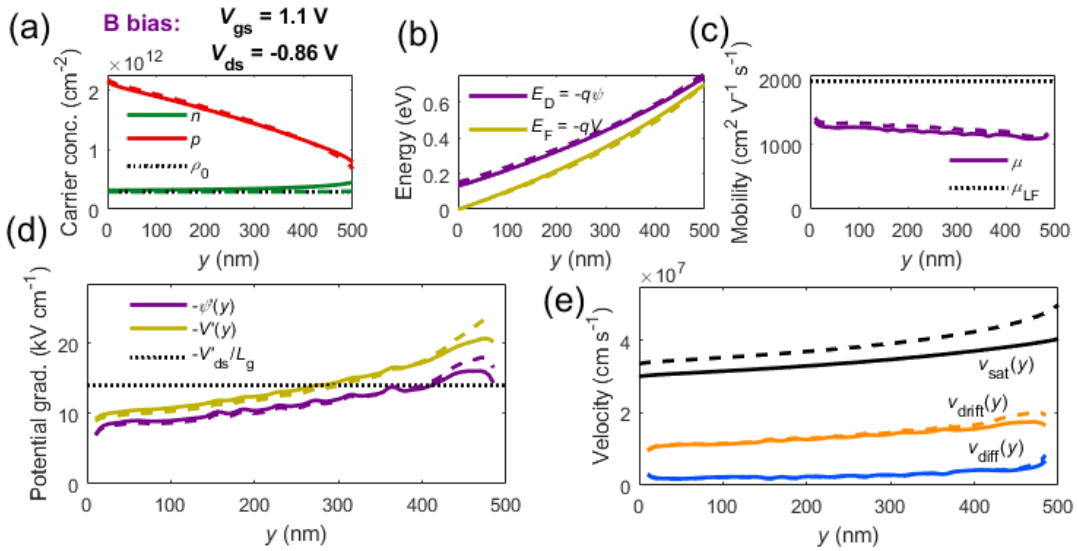

Fig. S3 Distribution along the channel of relevant parameters at bias point labelled as B in Fig. 6(a). Solid lines correspond to simulations with activated SHE (T = 571 K) and dashed lines to simulations with switched-off SHE (T = 300 K). (a) Electron and hole concentrations, (b) Dirac point and Fermi level, (c) field-dependent mobility (d) electric field and Fermi-level gradient, (e) saturation velocity and carrier velocity broken down into drift and diffusion velocities.

S4. Transfer characteristics

Fig. S4 shows the experimental transfer characteristic of the GFET (symbols). A fitting of the hole branch at low V_{ds} (represented by solid line) has been gotten by using a flatband voltage V_{gs0} = 2.19 V, puddle concentration $\rho_0 = 2.93 \cdot 10^{11}$ cm^{-2}, low-field mobility μ_{LF} = 1970 cm^2 V^{-1} s^{-1}, and contact resistance R_c = 11 Ω. The asymmetry in the experimental curve can be explained by the difference in mobilities of electrons and holes and/or the difference in contact resistances due to the formation of the p-n junction in the ungated regions.

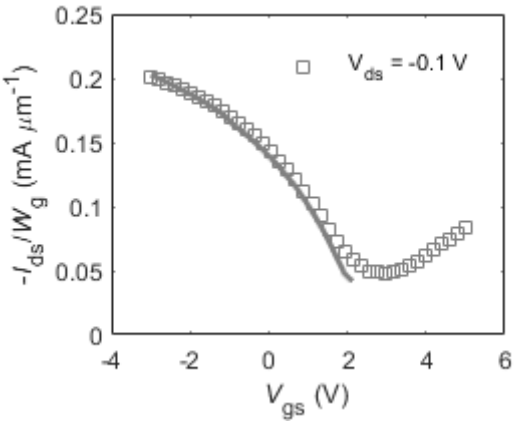

Fig. S4 Measured and simulated transfer curves for the GFET described in the main text.

S5. Small-signal parameters and RF performance determination

This section explains how the small-signal matrix $\boldsymbol{Y}(\omega)$ of the GFET is obtained from the stationary model explained in section S2. We consider here the two-port network in common-source configuration represented in Fig. S2(b) and we assume that the back gate has a negligible influence over the graphene charge given that the back gate capacitance is much smaller than the top gate capacitance. The charge at the gate, source and drain terminals (Q_g, Q_s and Q_d, respectively) can be obtained after the evaluation of the charge carrier distribution $q[p(y)$ -$n(y)]$. Upon application of a Ward-Dutton's linear charge partition scheme as the charge control model,[9] the terminal charges read as:

$$Q_\mathrm{d} = qW_\mathrm{g}\int_0^{L_\mathrm{g}} \frac{y}{L}[p(y)-n(y)]dy \tag{S16a}$$

$$Q_\mathrm{s} = qW_\mathrm{g}\int_0^{L_\mathrm{g}} \left(1-\frac{y}{L}\right)[p(y)-n(y)]dy \tag{S16b}$$

$$Q_\mathrm{g} = -qW_\mathrm{g}\int_0^{L_\mathrm{g}} [p(y)-n(y)]dy \tag{S16c}$$

Notice that the total charge in the device is zero, so the model is charge-conserving. From the charge model described above, the intrinsic capacitances of the equivalent circuit shown in Fig. S2(c), can be determined in the following way:

$$C_\mathrm{gg} = \left.\frac{\partial Q_\mathrm{g}}{\partial V'_\mathrm{gs}}\right|_{V'_\mathrm{ds}} \tag{S17a}$$

$$C_\mathrm{gd} = -\left.\frac{\partial Q_\mathrm{g}}{\partial V'_\mathrm{ds}}\right|_{V'_\mathrm{gs}} \tag{S17b}$$

$$C_\mathrm{dg} = -\left.\frac{\partial Q_\mathrm{d}}{\partial V'_\mathrm{gs}}\right|_{V'_\mathrm{ds}} \tag{S17c}$$

$$C_\mathrm{dd} = \left.\frac{\partial Q_\mathrm{d}}{\partial V'_\mathrm{ds}}\right|_{V'_\mathrm{gs}} \tag{S17d}$$

$$C_\mathrm{gs} = C_\mathrm{gg} - C_\mathrm{gd} \tag{S17e}$$

$$C_\mathrm{sd} = C_\mathrm{dd} - C_\mathrm{gd} \tag{S17d}$$

To complete the small-signal model, the transconductance g_m and output conductance g_sd need to be evaluated:

$$g_\mathrm{m} = \left.\frac{\partial I_\mathrm{ds}}{\partial V'_\mathrm{gs}}\right|_{V'_\mathrm{ds}} \tag{S18a}$$

$$g_\mathrm{sd} = \left.\frac{\partial I_\mathrm{ds}}{\partial V'_\mathrm{ds}}\right|_{V'_\mathrm{gs}} \tag{S18b}$$

As can be deduced from the diagram depicted in Fig. S2(c), the intrinsic admittance matrix then takes the form:

$$\boldsymbol{Y}'(\omega) = \begin{bmatrix} j\omega C_\mathrm{gg} & -j\omega C_\mathrm{gd} \\ g_\mathrm{m} - j\omega C_\mathrm{dg} & g_\mathrm{sd} + j\omega C_\mathrm{dd} \end{bmatrix} \tag{S19}$$

We must include the influence of the parasitic series resistances R_g, R_s and R_d (where R_g is the series resistance at the gate) and parasitic capacitances at the input C_pgs and output

C_{pds} of the two-port network, as can be observed in Fig. S2(d), to obtain the extrinsic admittance matrix $\boldsymbol{Y}(\omega)$. Then, we define the series resistance matrix $\boldsymbol{Z_c}$ and the parasitic capacitance matrix $\boldsymbol{C_p}$ as:

$$\boldsymbol{Z_c} = \begin{bmatrix} R_{\mathrm{g}} + R_{\mathrm{s}} & R_{\mathrm{s}} \\ R_{\mathrm{s}} & R_{\mathrm{d}} + R_{\mathrm{s}} \end{bmatrix} \tag{S20a}$$

$$\boldsymbol{C_p} = \begin{bmatrix} C_{\mathrm{pgs}} & 0 \\ 0 & C_{\mathrm{pds}} \end{bmatrix} \tag{S20b}$$

The extrinsic admittance matrix is calculated from the intrinsic one adding the effect of series resistances and parasitic capacitances as follows:

$$\boldsymbol{Y}(\omega) = \{[\boldsymbol{Y}'(\omega)]^{-1} + \boldsymbol{Z_c}\}^{-1} + j\omega\boldsymbol{C_p} \tag{S21}$$

From the elements of this complex matrix $\boldsymbol{Y}(\omega)$ we can extract frequency-dependent maximum current gain $h_{21}(\omega)$ and unilateral power gain $U(\omega)$:

$$h_{21}(\omega) = -\frac{y_{21}(\omega)}{y_{11}(\omega)} \tag{S22}$$

$$U(\omega) = \frac{|y_{21}(\omega) - y_{12}(\omega)|^2}{4\{\mathrm{Re}[y_{11}(\omega)]\mathrm{Re}[y_{22}(\omega)] - \mathrm{Re}[y_{12}(\omega)]\mathrm{Re}[y_{21}(\omega)]\}} \tag{S23}$$

In order to calculate the RF figures of merit, the cutoff frequncy $f_{\mathrm{T,x}}$ and the maximum oscillation frequency f_{max}, we evaluate $|h_{21}(\omega)|$ and $|U(\omega)|$ at low frequencies and then we extrapolate the curves so that $|h_{21}(2\pi f_{\mathrm{T,x}})| = 1$ and $|U(2\pi f_{\mathrm{max}})| = 1$.

It is usual to measure in the laboratory the S-parameters of a two-port network, that is, the matrix $\boldsymbol{S}(\omega)$,. Then it is convenient to add here the equations needed to transform the scattering parameters to the admittance parameters:

$$y_{11}(\omega) = Y_0 \frac{[1 - s_{11}(\omega)][1 + s_{22}(\omega)] + s_{12}(\omega)s_{21}(\omega)}{[1 + s_{11}(\omega)][1 + s_{22}(\omega)] - s_{12}(\omega)s_{21}(\omega)} \tag{S24a}$$

$$y_{12}(\omega) = Y_0 \frac{-2\, s_{12}(\omega)}{[1 + s_{11}(\omega)][1 + s_{22}(\omega)] - s_{12}(\omega)s_{21}(\omega)} \tag{S24b}$$

$$y_{21}(\omega) = Y_0 \frac{-2\, s_{21}(\omega)}{[1 + s_{11}(\omega)][1 + s_{22}(\omega)] - s_{12}(\omega)s_{21}(\omega)} \tag{S24a}$$

$$y_{22}(\omega) = Y_0 \frac{[1 + s_{11}(\omega)][1 - s_{22}(\omega)] + s_{12}(\omega)s_{21}(\omega)}{[1 + s_{11}(\omega)][1 + s_{22}(\omega)] - s_{12}(\omega)s_{21}(\omega)} \tag{S24b}$$

where $Y_0 = (50\ \Omega)^{-1}$.

S6. Parasitic capacitances

The experimental values of C_{pgs} and C_{pds} were extracted from the scattering parameters of an open structure (a device with same contact structure than the GFET but without a graphene layer) following a procedure described in ref. 10. Measurements are shown in Fig. S5.

In this work, we have extracted C_{pgs} and C_{pds} from the fitting of the GFET model to the experimental measurements of the admittance parameters. Fig. S5 shows the good agreement between the experimental values and the fitted ones.

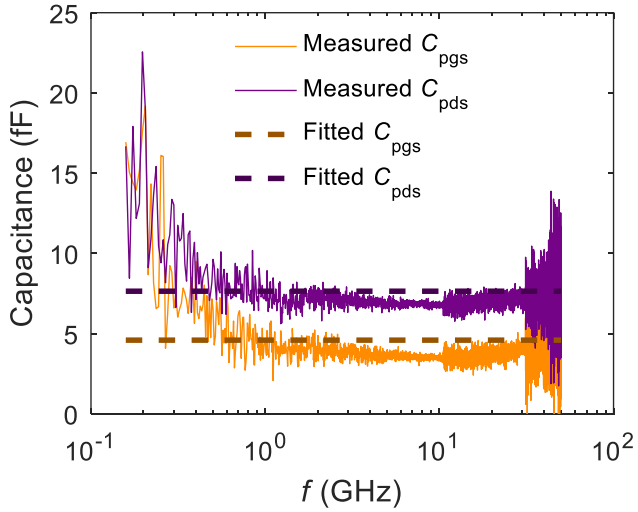

Fig. S5 Parasitic capacitances measured from the open structure of the GFET and their values obtained from *Y*-parameters fitting.

S7. Carrier distribution in the channel at maxima of $|g_m|$

Figure S6(c) shows the transconductance of the GFET considered in this work as a fuction of the extrinsic bias voltages V_{ds} and V_{gs}. The graph present labelled biases A, B, C and D that correspond to the biases where $|g_m|$ shows a local maximum. These biases roughly coincide with the maxima of f_{max}, as can be seen in Fig. 6(a) of the main text. It is interesting to study carrier distribution along the channel for these biases, so they are shown in Fig. S6(a), (b), (d) and (e). Biases A and B satisfy $V_{gs} < V_D$, so for both biases carriers in graphene are holes. In contrast, biases C and D are located in the electron branch ($V_{gs} > V_D$). For biases A and D, carriers are depleted close to the source while, for biases B and C, carriers are depleted close to the drain. Biases B and C present also a higher intrinsic voltage gain than A and D, as shown in Fig. 6(c) in the main text.

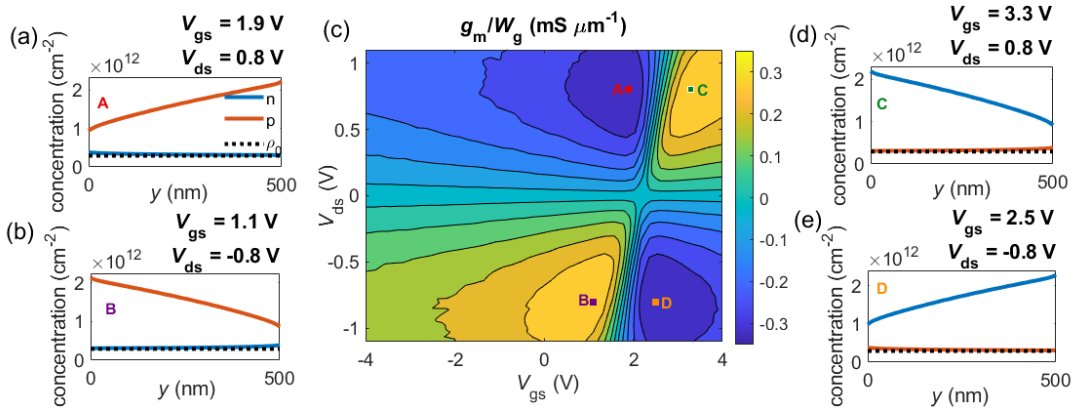

Fig. S6 Map of the bias-dependent transconductance. The map in (c) presents four maxima: (a) and (b) cases of a unipolar hole-dominated channel with the pinch-off point near the source and drain edge, respectively; and (d) and (e) cases of an electron-dominated channel near the drain and source edge, respectively. The labels A, B, C and D correspond to the bias location of the $|g_m|$ maxima.

S8. Effect of interface trap density

In this section we have analyzed the effect of the interface trap density on the DC and RF behavior. We have simulated the GFET with the parameters given in Table 1 of the main text with N_{it} = 0, 10^{12} and 10^{13} eV^{-1} cm^{-2}. Fig. S7 shows that the current-voltage curves simulated with N_{it} = 10^{12} eV^{-1} cm^{-2} do not differ significantly from the case without traps. The situation strongly changes for N_{it} = 10^{13} eV^{-1} cm^{-2}, where the high amount of charged defects clearly makes the carrier concentration at a given bias to decrease, which reduces the mobile charge and, thus, the total drain current. However, the highest possible $f_{T,x}$ and f_{max} that can be achieved considering any of the three examined N_{it} are quite similar. Fig. S8 presents the RF figures of merit as a function of the bias point, using the values of the parasitic elements of Table 2 in the main text. The maxima of $f_{T,x}$ and f_{max} reach approximately 25 and 40 GHz independently of N_{it} although they are located at different biases: as the density of defects grows, maxima move off from the Dirac voltage. It can thus be concluded that, in our model, N_{it} up to a level of 10^{12} eV^{-1} cm^{-2} does not influence the best RF performance of the GFET but it affects the bias that optimize it.

Notice that charged traps are assumed here to not change with the rapid variations of the small-signal voltage.[11] That is, the mean time of trapping and detrapping charges are larger than the period of the RF signal. In case that charged defects were affected by the small-signal voltage, RF performance would decrease considerably.

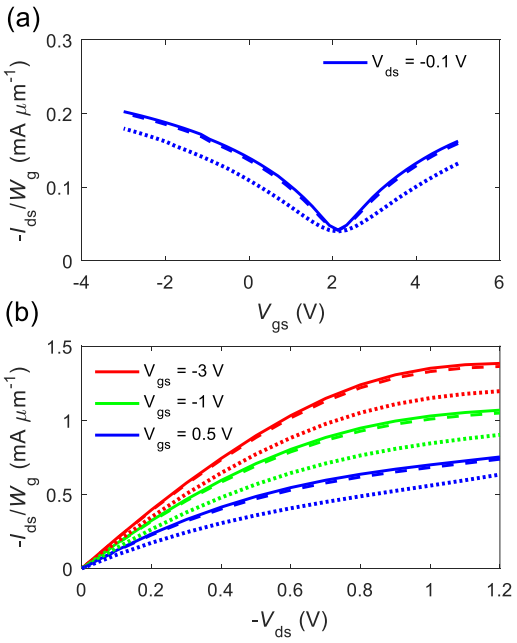

Fig. S7 Influence of interface trap density on the (a) transfer and (b) output curves. Solid lines correspond to N_{it} = 0 eV^{-1} cm^{-2}; dashed lines to N_{it} = 10^{12} eV^{-1} cm^{-2}; and dotted lines to N_{it} = 10^{13} eV^{-1} cm^{-2}.

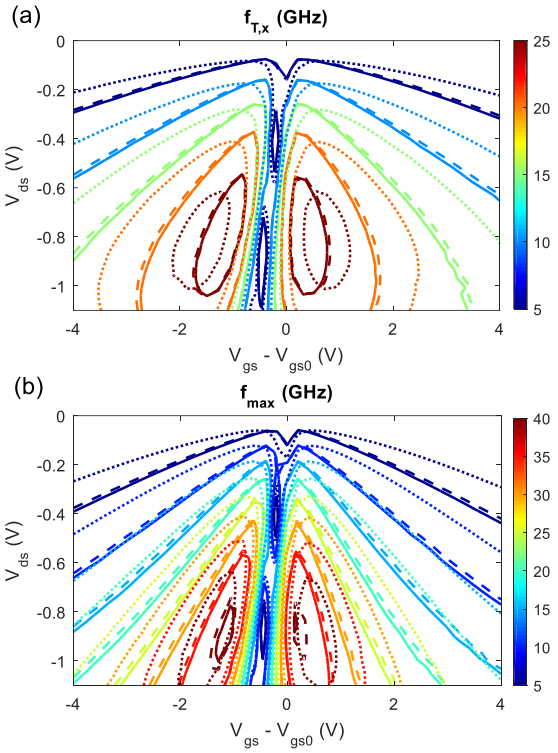

Fig. S8 Influence of the interface trap density on RF figures of merit: (a) $f_{T,x}$ and (b) f_{max}. Solid lines correspond to a N_{it} = 0 eV^{-1} cm^{-2}; dashed lines to N_{it} = 10^{12} eV^{-1} cm^{-2}; and dotted lines to N_{it} = 10^{13} eV^{-1} cm^{-2}.

S9. Effect of self-heating on f_{max}

We have compared the largest f_{max} that can be achieved with and without accounting the self-heating phenomena. The latter assumes that the thermal resistance is null, so graphene channel remains at room temperature. Fig. S9 shows the bias dependence of f_{max} in both cases, showing that self-heating severely limit RF performance of GFETs. Specifically, f_{max} over 60 GHz can be reached for the studied bias window considering that the device operates at room temperature.

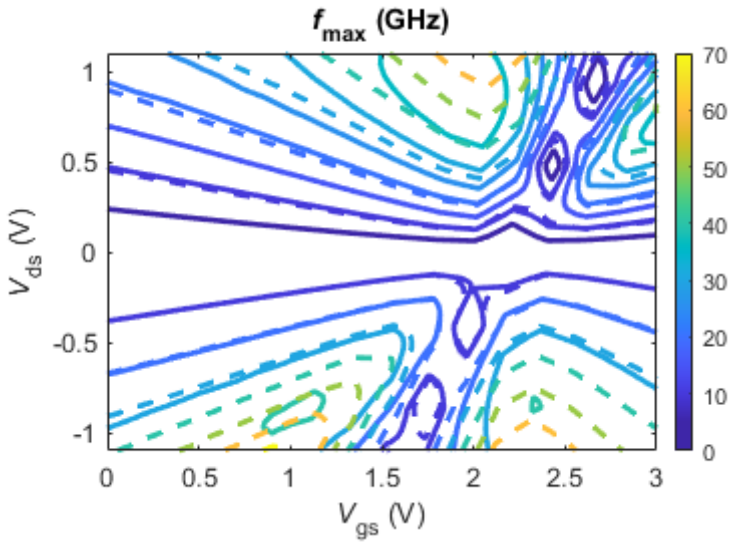

Fig. S9 Map of f_{max} as a function of the bias point for GFET including the self-heating effect (solid lines) and switching off such a phenomena (dashed lines).

References

1 M. Bonmann, M. Asad, X. Yang, A. Generalov, A. Vorobiev, L. Banszerus, C. Stampfer, M. Otto, D. Neumaier and J. Stake, *IEEE Electron Device Lett.*, 2019, **40**, 131–134.

2 S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, John Wiley & Sons, INC, Hoboken, NJ, 3rd edn.

3 S. J. Mason, *Trans. IRE Prof. Gr. Circuit Theory*, 1954, **CT-1**, 20–25.

4 M. S. Gupta, *IEEE Trans. Microw. Theory Tech.*, 1992, **40**, 864–879.

5 P. C. Feijoo, D. Jiménez and X. Cartoixà, *2D Mater.*, 2016, **3**, 025036.

6 F. Rana, *Phys. Rev. B*, 2007, **76**, 155431.

7 F. Rana, P. A. George, J. H. Strait, J. Dawlaty, S. Shivaraman, M. Chandrashekhar and M. G. Spencer, *Phys. Rev. B - Condens. Matter Mater. Phys.*, 2009, **79**, 115447.

8 K. Nagashio, T. Nishimura and A. Toriumi, *Appl. Phys. Lett.*, 2013, **102**, 173507.

9 Y. Tsividis and C. McAndrew, *The MOS transistor*, Oxford University Press, New York, Third Edit., 2012.

10 G. Dambrine, A. Cappy, F. Heliodore and E. Playez, *IEEE Trans. Microw. Theory Tech.*, 1988, **36**, 1151–1159.

11 H. Ramamoorthy, R. Somphonsane, J. Radice, G. He, J. Nathawat, C.-P. Kwan, M. Zhao and J. P. Bird, *Semicond. Sci. Technol.*, 2017, **32**, 084005.