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Supplementary Information: Multiple Negative Differential Resistance Phenomenon in Vertical Tunneling Device Based on Double van der Waals Heterojunction

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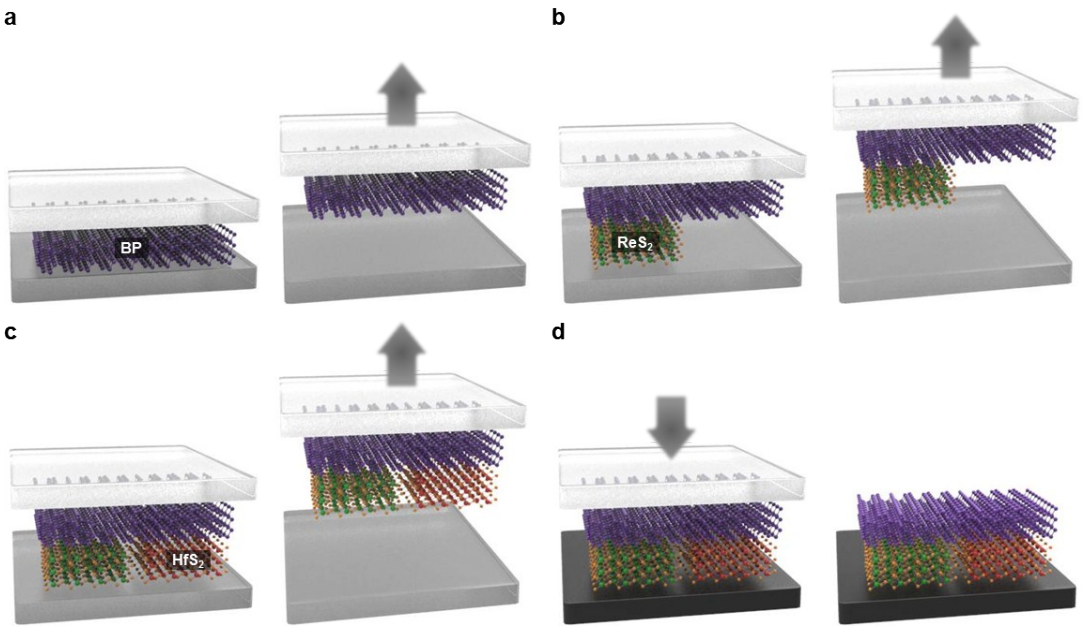

Figure S1. Residue-free transfer method employing the difference in adhesion force between materials. **(a)** Picking up the BP flake with the polymer layer **(b-c)** Picking up the ReS_2 and HfS_2 flakes **(d)** Transfer of the BP/(ReS_2+HfS_2) structure onto the SiO_2/Si substrate.

Figure S1 shows the residue-free transfer process employing the difference in adhesion force between materials. First, flakes of black phosphorus (BP), rhenium disulfide (ReS_2) and hafnium disulfide (HfS_2) were mechanically exfoliated onto clean substrates using a tape-based exfoliation method. Then, a polymer layer was prepared and contacted onto the exfoliated BP flake using a micromanipulator (Figure S1 a). Because the adhesion force between the polymer layer and the BP flake is stronger than that between the exfoliated BP flake and the substrate, the BP flake was attached to the polymer layer and then lifted off from the substrate. Similarly, the ReS_2 and HfS_2 flakes were contacted onto the surface of the BP flake and lifted up because of stronger adhesion forces at the BP/ReS_2 and BP/HfS_2 interfaces than those at the substrate/ReS_2 and substrate/HfS_2 interfaces, respectively (Figure S1 b,c). Next, the BP/(ReS_2+HfS_2) heterostructure underneath the polymer layer was transferred onto the desired area in the SiO_2/Si

substrate (Figure S1 d). Finally, the transferred heterostructure was cleaned in acetone during 2 hours to remove polymer residuals, followed by rinsing in isopropyl alcohol (IPA) and deionized water (DI) to remove acetone residuals. This method ensures residue-free BP/ReS_2 and BP/HfS_2 interfaces which are essential to achieve a reliable tunneling device.

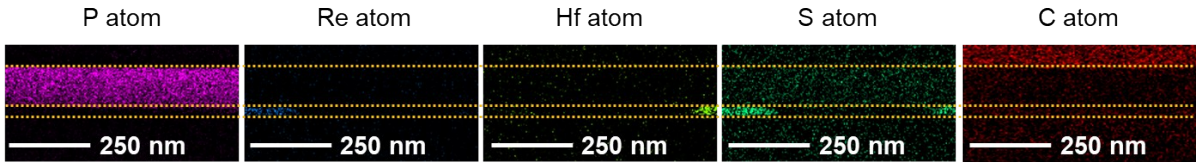

Figure S2. Energy-dispersive X-ray spectroscopy (EDS) mapping images

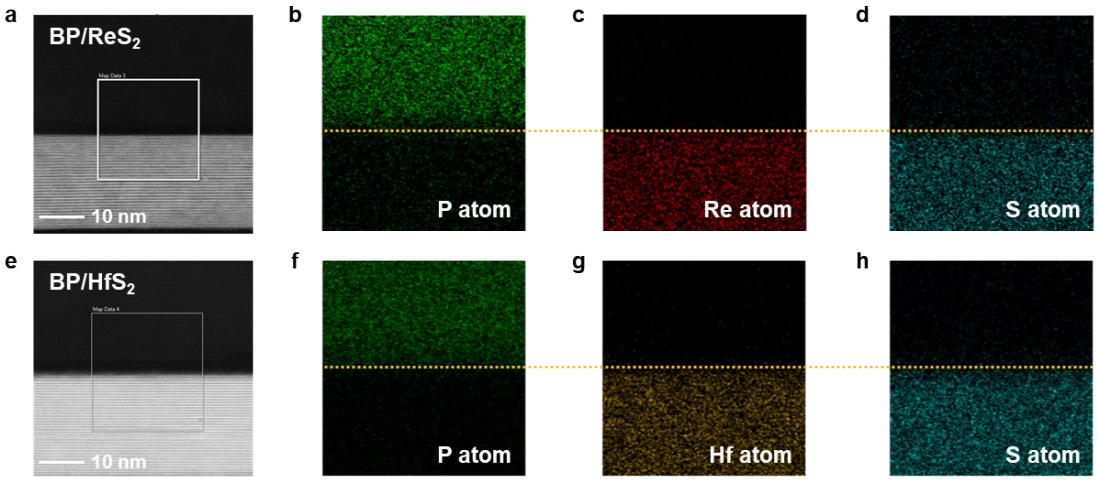

Figure S3. EDS elemental mappings near heterojunction interfaces. **(a-d)** Mapping of P, Re, S atoms near the BP/ReS_2 heterojunction interface **(e)-(h)** Mapping of P, Re, S atoms near the BP/HfS_2 heterojunction interface.

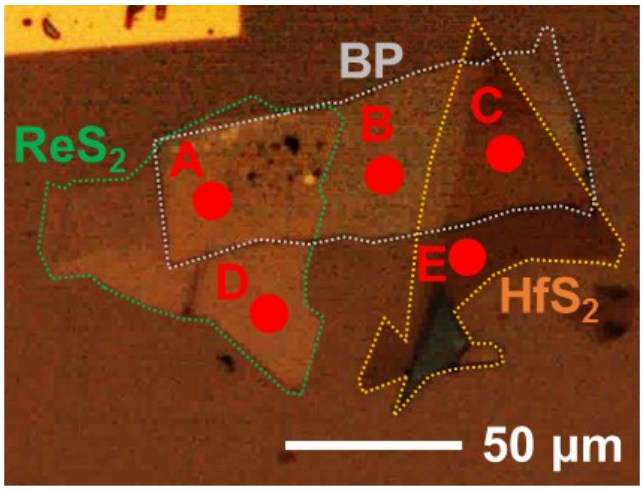

Figure S4. Optical image of the BP/(ReS_2+HfS_2) double heterojunction used for the μ-XPS measurements. The red circles indicate the spots illuminated by X-ray beam of 10 μm diameter.

Figure S4 shows the optical image of the BP/(ReS_2+HfS_2) heterojunction on the Si/SiO_2 substrate, which was used for the μ-XPS measurements. Red circles indicate the regions irradiated by the X-ray beam of 10 μm diameter, where core-level (CL) spectra were obtained. To acquire reliable CL information at the heterojunction regions (A and C regions), we used the residue-free transfer method introduced in Figure S1. In contrast to the structure of the vertical device (BP is stacked on the ReS_2 and HfS_2), ReS_2 and HfS_2 are stacked on the BP because the thin layered BP is very unstable in air. Particularly, to obtain the CL spectra of BP and ReS_2 (or HfS_2) simultaneously at the heterojunction regions, sufficiently thin ReS_2 (3.2 nm) and HfS_2 (2.8 nm) flakes were used to fabricate the double heterojunction. If the upper n-type materials (ReS_2 and HfS_2) are too thick, then the CL spectrum from the lower BP cannot be obtained because the photo-emitted electrons escaped from the lower BP cannot pass through the upper n-type materials and reach the electron energy analyzer. Although the thickness of the TMD flakes used for the μ-XPS measurements is smaller than those used in the vertical device, the band alignments of BP/ReS_2 and BP/HfS_2 junctions would not be changed much. According to a

previous study[9], the band structure of a monolayer ReS_2 is almost the same as that of bulk ReS_2. Furthermore, the band gap of 4–5 layered HfS_2 is almost the same as that of bulk HfS_2 (monolayer HfS_2: ~1.18 eV; bulk HfS_2: ~1.1 eV), and the Fermi-level of HfS_2 is constant regardless of the flake thickness[2]. Because the charge transfer in the heterojunction only occurs until the Fermi levels of the two materials become equal, the charge transfer between BP and 4–5 layered n-type TMD materials would be similar to that between BP and 20 nm-thick n-type TMD materials.

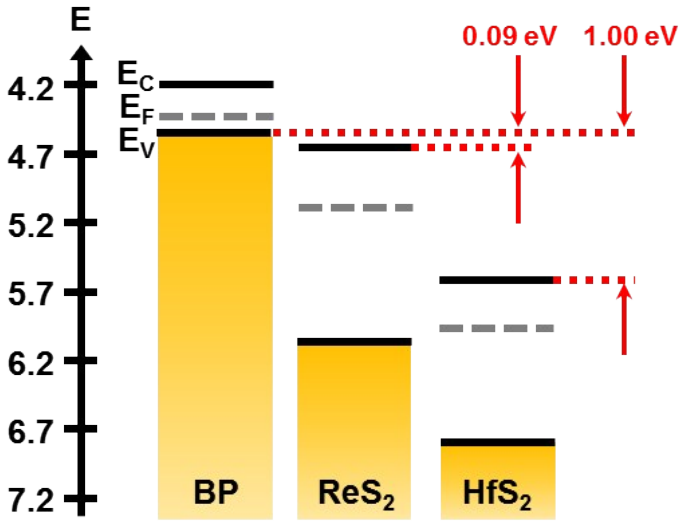

Figure S5. Energy band diagrams for BP, ReS_2 and HfS_2 derived the from first-principle calculations[1-5].

Figure S5 shows the energy band alignments for BP, ReS_2 and HfS_2 obtained by the first-principle calculations[1-5]. The conduction band minimum (valence band maximum) values of BP, ReS_2 and HfS_2 are 4.2 (4.59), 4.68 (6.05) and 5.59 (6.83) eV, respectively. The band gap values of BP, ReS_2 and HfS_2 are 0.39, 1.37 and 1.23 eV, respectively. Thus, the estimated broken energy gaps of BP/ReS_2 and BP/HfS_2 junctions are 0.09 and 1.00 eV. By selecting such 2D

materials properly, the type-III heterojunction can be easily formed without any additional electrical or chemical doping process.

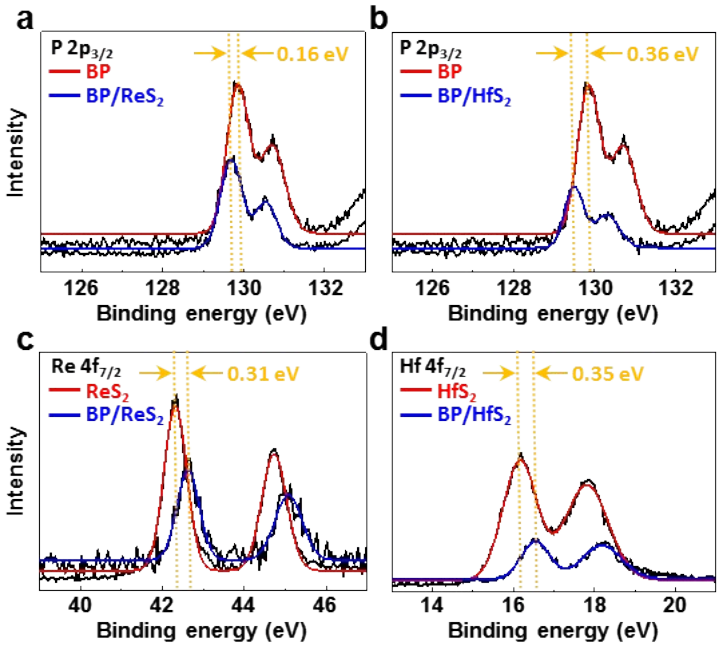

Figure S6. Comparison of core-levels (a) P $2p_{3/2}$ peak in BP and BP/ReS_2 (b) P $2p_{3/2}$ peak in BP and BP/HfS_2 (c) Re $4f_{7/2}$ peak in ReS_2 and BP/ReS_2 (d) Hf $4f_{7/2}$ peak in HfS_2 and BP/HfS_2

Figure S6 shows the high-resolution core-level spectra obtained at the regions indicated by the red circles in Supplementary Figure S4. The binding energy of P $2p_{3/2}$ core level in the BP/ReS_2 (BP/HfS_2) heterostructure was lower by 0.16 eV (0.36 eV) compared to that in individual BP [shift from 129.86 to 129.67 eV (129.50 eV)]. In contrast, the Re $4f_{7/2}$ and Hf $4f_{7/2}$ core level in heterostructures showed higher binding energies by 0.31 and 0.35 eV, respectively (shift from 42.35 to 42.66 eV for Re $4f_{7/2}$, and from 16.17 to 16.52 eV for Hf $4f_{7/2}$).

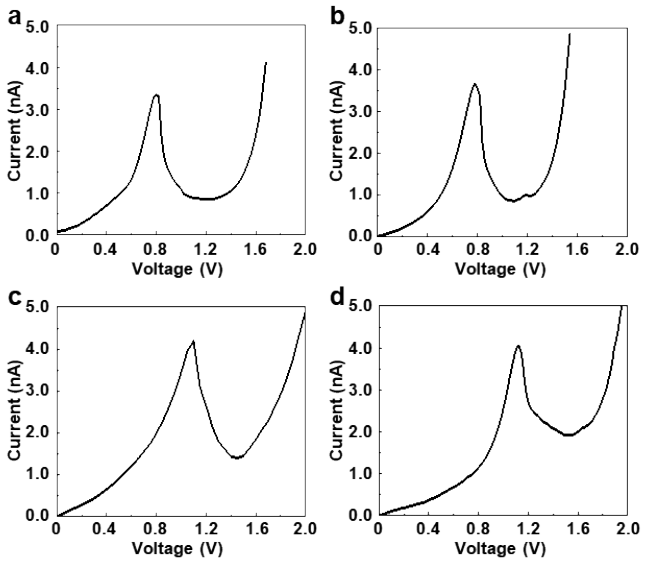

Figure S7. Current-voltage characteristics of single heterojunction devices (single-peak NDR). **(a-b)** BP/ReS_2 devices **(c-d)** BP/HfS_2 devices. The parameters extracted from these curves can be found in Table S1.

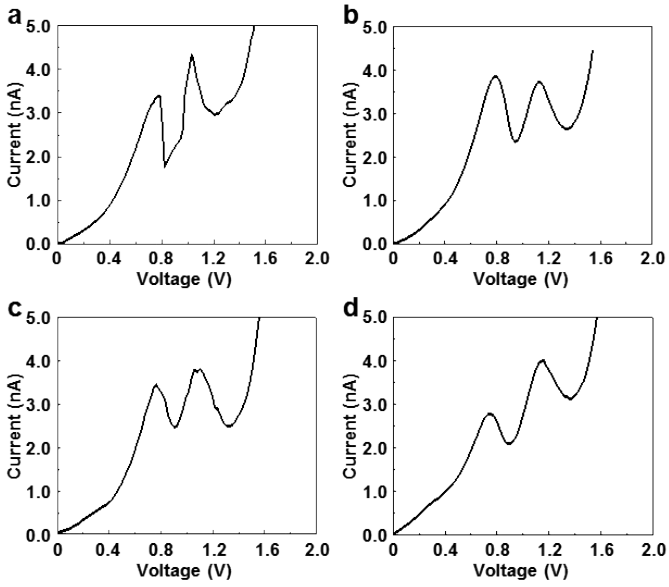

Figure S8. (a-d) Current-voltage characteristics of double heterojunction devices (multi-peak NDR). The parameters extracted from these curves can be found in Table S2.

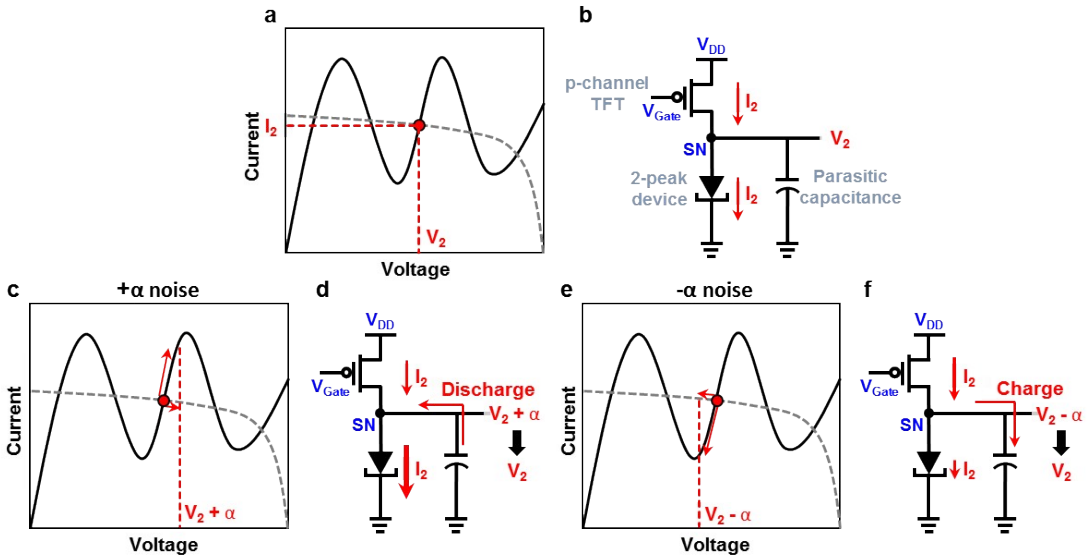

Figure S9. Load line configuration and equivalent circuit of the ternary latch (a-b) without voltage fluctuation at the storage node (SN). (c-d) with voltage fluctuation of +α at the SN. (e-f) with voltage fluctuation of –α at the SN. The red arrows represent the magnitude of the current flowing through the components.

Figure S9 illustrates how the states stored in the latch can be stably maintained through the self-latching operation. Supplementary Figure 9a,b show the load line configuration and equivalent circuit when the voltage of the SN is settled to V_2 without voltage fluctuations. Here, the voltage drops across TFT and 2-peak device are V_{DD}-V_2 and V_2, respectively, and the same amount of current (I_2) flows through the TFT and 2-peak devices. However, as shown in Figure S9 c,d, if the voltage variation of α occurs at the SN due to the leakage of charge into the parasitic capacitance, the voltage across the TFT decreases to (V_{DD}-V_2-α) and that across the 2-peak device increases to (V_2+α). Therefore, the current through the TFT decreases and that through the 2-peak device increases. This current discontinuity induces another current flowing from the parasitic capacitance into the 2-peak device, subsequently reducing the amount of

charges stored in the parasitic capacitance. As a result, the SN voltage is settled back to the V_2 (Figure S9 d). Similarly, a voltage fluctuation from V_2 to V_2-α is also recovered to V_2.

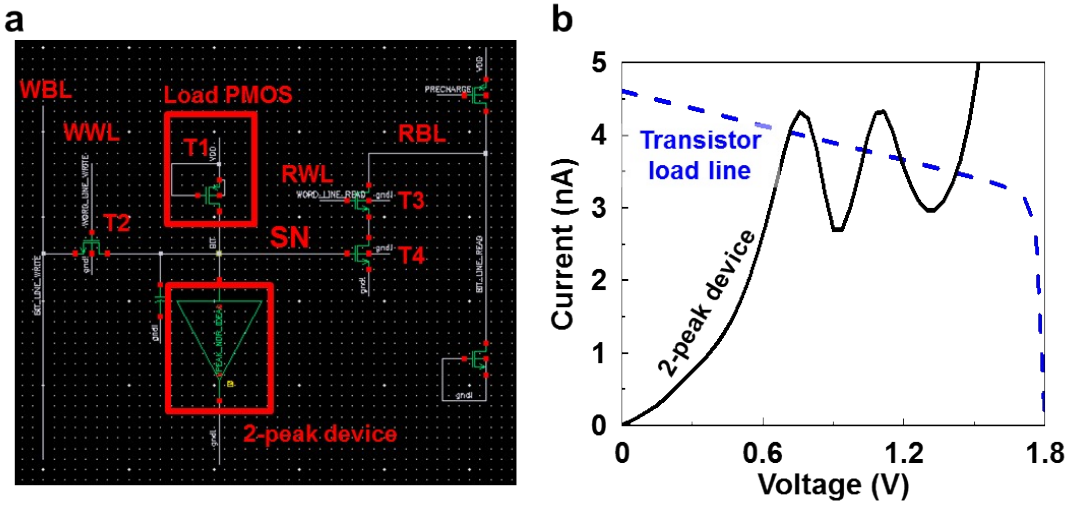

Figure S10. (a) The configuration of the designed ternary SRAM circuit. (b) The I-V curve of the 2-peak device driven by experimental NDR data and the load line of the PMOS transistor. The detailed specifications of transistors used in the simulation are given in Table S4.

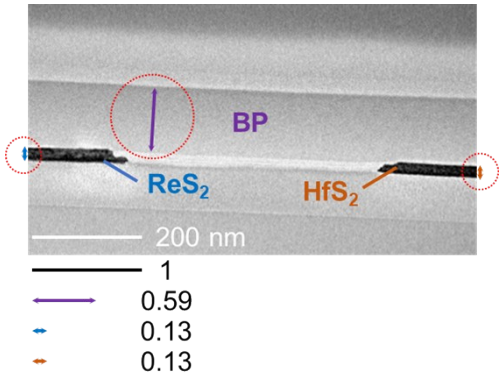

Figure S11. Thickness of the BP, ReS_2 and HfS_2 flakes.

Figure S11 shows an X-TEM image of the BP/(ReS_2+HfS_2) heterojunction. In the figure, the arrows denote the thickness of the BP, ReS_2 and HfS_2 flakes. The length of the arrows was

normalized by the length of the scale bar, and the normalized lengths are provided below the image. By multiplying the normalized lengths by 200 nm, we could infer the thickness of the BP, ReS_2 and HfS_2 flakes as 118, 26, and 26 nm, respectively.

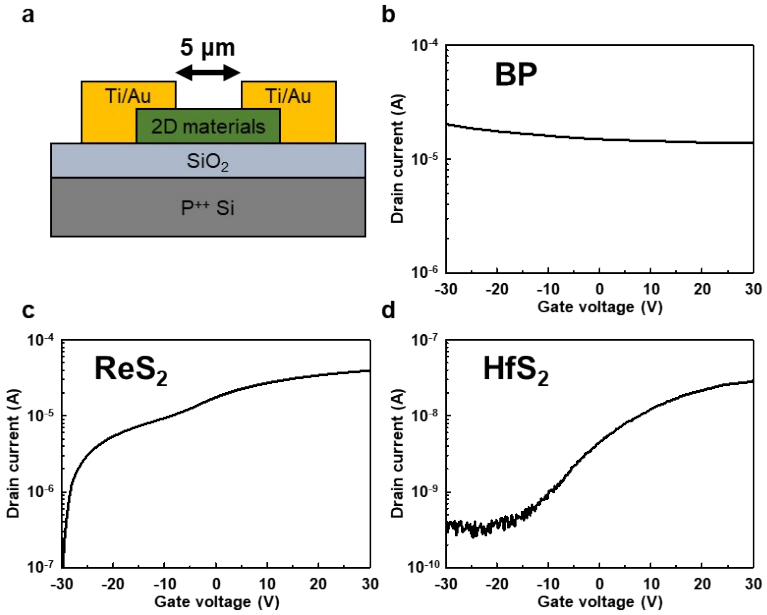

Figure S12. (a) Schematic of the thin-film transistor (TFT) fabricated with 2D materials. I_D-V_G characteristic curves of: (b) BP TFT, (c) ReS_2 TFT, and (d) HfS_2 TFT

As shown in Figure S12, the TFTs fabricated with BP and ReS_2 are highly conductive. As such, their channel resistances are very low, and would hardly affect the m-NDR phenomenon. On the other hand, the relatively low conductivity of HfS_2 makes the voltage drop across the HfS_2 flake not negligible, which is expected to cause subtle variations of m-NDR characteristics, such as the position of the peak current, the difference in the 1st and the 2nd peak positions, and the PVCR, as shown in Figures S7 and S8 in the Supporting Information.

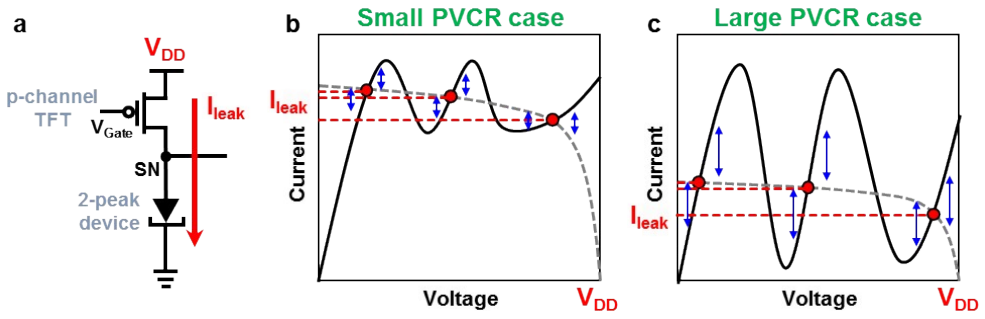

Figure S13. (a) Schematic of a ternary latch circuit. Load line configuration of the ternary latch circuit using an m-NDR device with: (b) a small PVCR or (c) a large PVCR

The peak-to-valley ratio (PVCR) of the m-NDR device based on the BP/(ReS_2+HfS_2) junction was relatively small (<2) compared to the values (~4 and ~3, respectively) of BP/ReS_2 and BP/HfS_2 NDR devices. In the context with an MVL circuit, it is advantageous to use an NDR device with a large PVCR value for the following reasons. First, the static power of the MVL circuit, which is calculated by multiplying V_{DD} and I_{leak}, can be lowered by using the NDR device with a large PVCR. This is because the operating points (red dots) are formed at lower current levels (red dotted lines). Second, the restoring current (blue arrows), which is related to the immunity to the noise, can be much increased if the NDR device with a large PVCR is used for the MVL circuit. Therefore, increasing the PVCR of the m-NDR device would be an important task in the future.

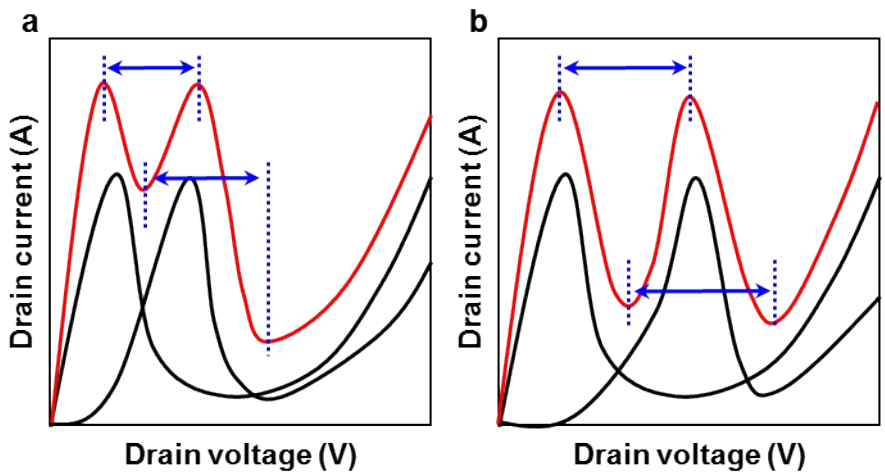

Figure S14. Double NDR characteristic curves with (a) a narrow gap between 1st and 2nd peak/valley and (b) a broad gap between 1st and 2nd peak/valley

By controlling the 1st and/or 2nd NDR characteristic curves, it is possible to tune the voltage and current range between NDR peak and valley, and that between first valley and second peak**.** For this NDR peak/valley engineering, we propose three strategies as described below.

i. First is to modulate the broken energy gap of heterojunction. As we proved in our study (Figure 3), the voltage and current of the peak and valley points increase (all peak and valley points are right- and up-shifted) when a broken energy gap becomes larger. In a previous study[10], a broken energy gap of MoS_2/WSe_2 heterojunction was modulated via the application of dual gate voltages to MoS_2 and WSe_2. The peak and valley points were also right- and up-shifted by applying a higher gate voltage (same trend as our results).

ii. Second is to control metal-semiconductor contact resistance (R_c). The R_c control changes the voltage dropped to the heterojunction, consequently adjusting the NDR peak and

valley points. A gated graphene-semiconductor (GS) can be considered as the controllable contact for this NDR peak/valley engineering.

iii. Third is to use materials with different resistivity or dimension, as shown in Figure S12 in Supporting Information. Through selection of materials, doping techniques, and dimension control, it is possible to change the sheet resistance of materials and thereby the NDR characteristic curves.

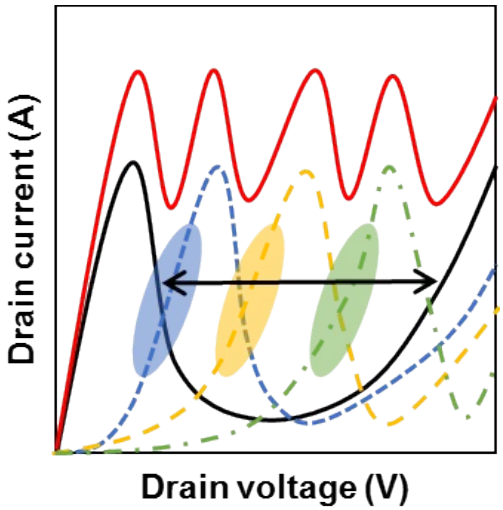

Figure S15. Sequential quadruple-negative differential resistance characteristic curves.

More than two NDR peaks can be achieved by forming multiple heterojunctions. For this, two conditions are required as follows. First, as shown in Figure S14, "1st threshold voltages (V_{TH}, oval-shaped regions)" of the second and next NDR devices have to appear between "NDR region" and "2nd V_{TH}" of the first NDR device (indicated by a black arrow). Second, the current level of NDR devices has to be similar such that all peaks appear.

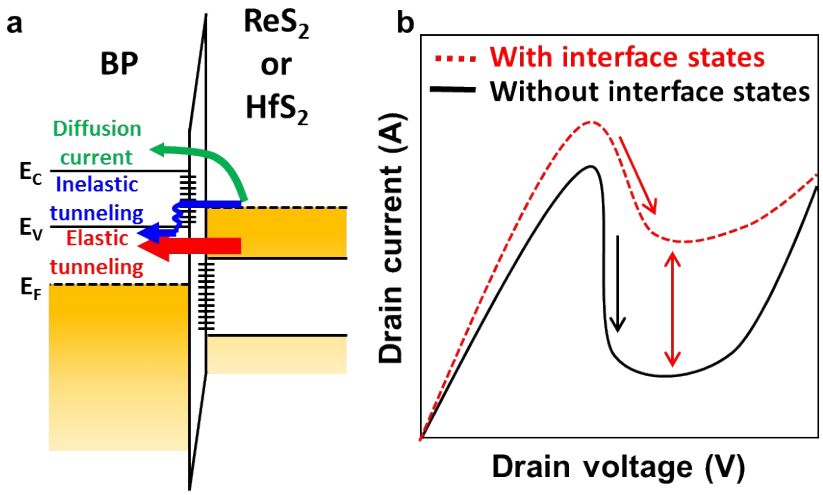

Figure S16. (a) Energy band diagram of heterojunction under a positive bias. (b) NDR characteristic curves with and without interface states.

Ideally, 2D materials have a pristine surface, but in reality, there are surface point defects like vacancies and interstitials. The interface trap states based on such point defects increases inelastic tunneling current (blue arrow in Fig. S16) via the Shockley-Read-Hall (SRH) recombination of majority carriers[10,11]. This inelastic current contributes to the total current together with the elastic tunneling current (a red arrow) that was only considered in ideal heterojunction device model. Following are the equations of elastic and inelastic tunneling currents[10,11].

$$I_{tunnel} = \frac{2\pi\alpha q}{h}\int_{E_{C_{MS2}}}^{E_{V\_BP}} DOS_{BP}(E) \times DOS_{MS2}(E) \times [f_{BP}(E) - f_{MS2}(E - qV)]dE \quad \text{(Elastic tunneling)},$$

where q is the elementary charge, h is Planck's constant, E_{V_BP} is the valence band maximum energy in BP, α is the fitting parameter, E_{C_MS2} is the conduction band minimum energy in MS_2 (M represents a transition metal such as Re or Hf), and V is the applied voltage. $DOS_{BP}(E)$ and $DOS_{MS2}(E)$ represent the density of states of BP and MS_2, respectively, and $f_{BP}(E)$ and $f_{MS2}(E)$ represent the density of states and the Fermi–Dirac distribution functions of BP and MS_2, respectively.

$$I_{SRH} = q\frac{np - n_0 p_0}{\tau(n+p)} \qquad \text{(Inelastic tunneling)},$$

where τ is tunneling-assisted recombination life time, n and p are the electron and hole density of n-type and p-type materials near the junction interface, respectively. n_0 and p_0 are electron and hole density of n-type and p-type materials at bulk, respectively.

The total tunneling current is the sum of I_{tunnel} and I_{SRH}, and consequently, the characteristics of NDR curve are changed as shown in Figure S16(b). Because the total tunneling current continuously flows through the trap states in the BP band gap rather than being completely blocked by the BP band gap, the current level at the NDR region falls slowly. In addition, I_{SRH} makes the valley current increase, reducing the peak-to-valley ratio that is an important figure of merit of NDR device. If the density of the trap states is significantly high, the NDR curve can disappear[12,13]. However, the density of interface trap states in BP (6.08×10^{11} $cm^{-2}eV^{-1}$), HfS_2 (6×10^{11} $cm^{-2}eV^{-1}$), and ReS_2 (not yet known) is comparatively smaller than silicon (10^{13}-10^{14} $cm^{-2}eV^{-1}$)[14,15], and thus the NDR curve is well observed in room temperature.

Table S1. The parameters of current-voltage characteristics of BP/ReS_2 and BP/HfS_2 single heterojunction devices.

Heterojunction type and data set	Peak voltage (V)	PVCR (A/A)	FWHM (V)
BP/ReS_2 (Figure S7a)	0.80	3.88	0.23
BP/ReS_2 (Figure S7b)	0.78	4.26	0.24
BP/HfS_2 (Figure S7c)	1.10	2.99	0.44
BP/HfS_2 (Figure S7d)	1.12	2.11	0.48

Table S2. The parameters of current-voltage characteristics of $BP/(ReS_2+HfS_2)$ double heterojunction devices.

Data from	1st peak voltage (V)	2nd peak voltage (V)	Voltage difference between 1st and 2nd peaks (V)	PVCR of the 1st peak	PVCR of the 2nd peak
Figure S8a	0.79	1.03	0.24	1.94	1.47
Figure S8b	0.79	1.12	0.33	1.64	1.41
Figure S8c	0.77	1.10	0.33	1.40	1.53
Figure S8d	0.76	1.14	0.38	1.34	1.29

Table S3. The parameters used in the analytic NDR device model. The vdW material properties were referred to previous literatures[6-8].

Parameters	BP	ReS_2	HfS_2
CBM (E_C)	4.2 eV	4.7 eV	5.0 eV
VBM (E_V)	4.6 eV	6.07 eV	6.6 eV
Fermi-level (E_F)	4.5 eV	5.1 eV	5.2 eV
Band gap (E_g)	0.4 eV	1.37 eV	1.1 eV

Effective mass (m*)	2.71×10^{-31} kg	7.56×10^{-31} kg	2.18×10^{-31} kg
Density of states (DOS)	$(4\pi m^*)/h^2$		
Fermi-Dirac distribution function (f(E))	$(1+\exp[(E-E_F)/k_BT])^{-1}$		

Table S4. The specification of transistors used in the ternary SRAM circuit model

Transistor	Width (nm)	Length (nm)	V_{TH} (mV)
T1	600	400	463
T2	420	500	84
T3	220	180	484
T4	220	180	484

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