Electronic Supplementary Material (ESI) for Nanoscale.

High Sensitivity Ultraviolet Detection Based on Three-Dimensional Graphene Field Effect Transistors Decorated with TiO_2 NPs

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Supplementary Materials

1. The detailed fabrication process of the 3D GFETs decorated with TiO_2 NPs

The detailed fabrication process of the three-dimensional (3D) graphene field-effect transistor (GFET) decorated with TiO_2 NPs is shown below point by point (**Figure S1**):

(a) After a 15-minute dip in H_2O_2 and H_2SO_4 solution (volume ratio 1:4) at 85 °C, the Si wafer was rinsed with deionized water and dried with N_2 gas. Magnetron sputtering and lift-off processes were conducted successively to pattern the 50-nm-thick Al sacrificial layer.

(b) The strained SiN_x layers were deposited on the Al sacrificial layer by a STS mixed frequency nitride plasma-enhanced chemical vapor deposition (PECVD) system, which consisted of a compressive trained SiN_x layer at the bottom and a tensile strained SiN_x layer on the top, with thicknesses of 120 nm and 80 nm, respectively. After the deposition step, reactive ion etching (RIE) process was performed to pattern the strained SiN_x layers.

(c) Magnetron sputtering and lift-off processes were performed to pattern the Cr/Au (thicknesses of 10 nm/30 nm) gate electrode on the strained SiN_x layers.

(d) A layer of SiO_2 with the thickness of 30 nm was deposited on the gate electrode to realize a buried-gate structure, using PECVD process. Then, RIE etching process was conducted to pattern the dielectric layer.

(e) A monolayer graphene was transferred onto the top of the dielectric layer. Then, O_2 plasma etching process was performed to pattern the graphene layer.

(f) Electron beam evaporation and lift-off processes were conducted to pattern the Cr/Au (thicknesses of 10 nm/50 nm) source and drain electrodes on top of the graphene layer. Within this step, the planar (two-dimensional, 2D) buried-gated GFET was obtained.

(g) Upon selective etching of the Al sacrificial layer using $FeCl_3$ solution, the highly strained SiN_x layers rolled the 2D GFET into a 3D tubular architecture.

(h) After being rinsed in deionized water and dried out naturally, the 3D GFET was obtained.

(i) The TiO_2 NPs are deposited on graphene conductive channel by introducing the TiO_2 NPs solution at one end of the tubular 3D GFET, and it would sucked into the hollow-core tube towards the graphene conductive channel region, due to the large capillary force.

(j) After being dried out in the air, the 3D GFETs decorated with TiO_2 NPs were obtained.

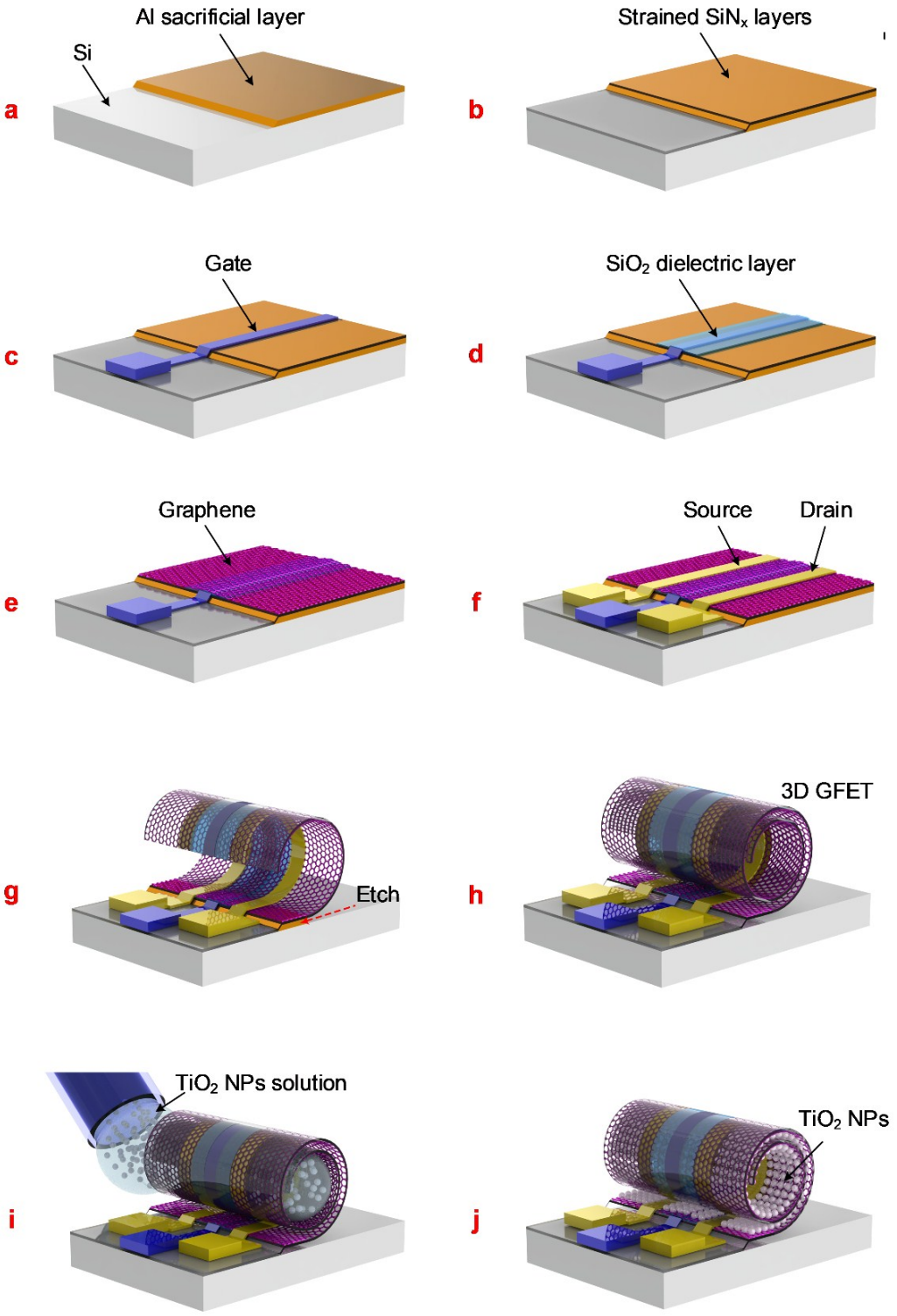

Figure S1 The fabrication process of 3D GFETs with TiO_2 NPs decoration. (a) Sputter Al sacrificial layer on Si substrate. (b) Deposit strained SiN_x layers. (c) Sputter Cr/Au gate electrode. (d) Deposit SiO_2 dielectric layer. (e) Transfer and pattern the monolayer graphene. (f) Evaporate Cr/Au source and drain electrodes. (g) Selectively etch the Al sacrificial layer. (h) Rinse and dry

out the 3D GFET. (i) Decorate the 3D GFET with TiO_2 NPs. (j) Dry out the TiO_2 NPs decorated 3D GFET in the air.

2. EDS spectra of the TiO_2 NPs decorated 3D GFET

The energy dispersive X-ray spectroscopy (EDS, Quanta 200 ESEM FEG, FEI, OR, USA) was employed to confirm the existence of TiO_2 in the conductive channel of the 3D GFETs with TiO_2 NPs decoration. As shown in **Fig. S2b-S2d**, the O and Ti elements were detected at different positions of the conductive channel of the device labeled by red boxes in **Fig. S2a**. These results verify not only the existence of the TiO_2 NPs but also the distribution of the TiO_2 NPs throughout the conductive channel. The Cl element was from the $TiCl_4$ solution, which was used in the preparation process of TiO_2 NPs with a sol-gel method [1].

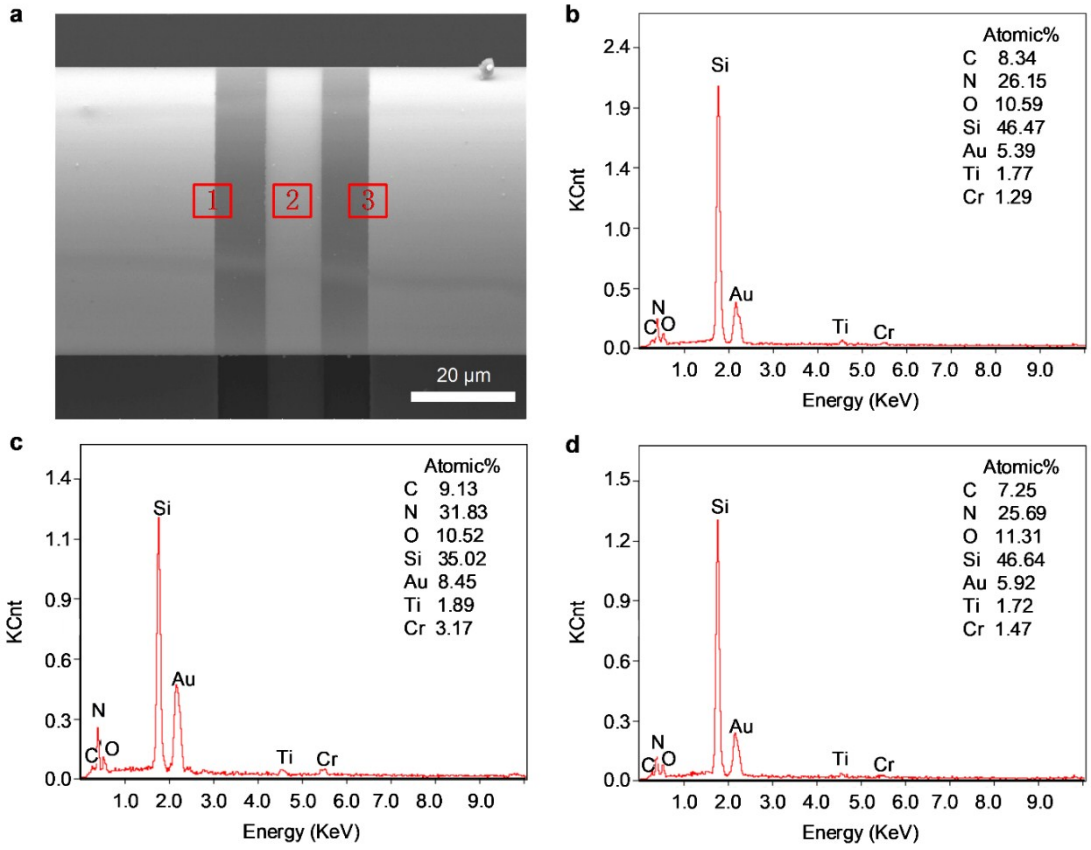

Figure S2 EDS spectra of the conductive channel of the 3D GFET with TiO_2 NPs decoration. (a) Zoomed-in details of the graphene conductive channel. (b)-(d) The EDS spectra of the

conductive channel of the 3D GFET with TiO_2 NPs decoration, at different positions labeled 1, 2 and 3 in (a), respectively.

3. The field effect mobility and metal-graphene contact resistance of the 3D GFET without and with TiO_2 NPs decoration

The transfer characteristics of the 3D GFET without and with TiO_2 NPs decoration were measured at room temperature and under ambient conditions. Figure S3 shows the total resistance (R_{total}) of the 3D GFET before and after coating TiO_2 NPs as a function of gate voltage (V_{gs}) at a source-drain bias (V_{ds}) of 1 V. In order to obtain the carrier mobility (μ) and contact resistance ($R_{contact}$) from the measured data of **Fig. S3**, we adopt a model proposed by Kim *et al*. [2] to analyze the resistive behavior of the 3D GFETs without and with TiO_2 NPs decoration. The R_{total} profiles can be fitted to the equation [2]

$$R_{total} = R_{contact} + R_{channel} = R_{contact} + \frac{1}{\mu e\sqrt{n_0^2 + n^2}}\frac{L}{W} \quad (1)$$

where $R_{channel}$ is the resistance of the graphene channel, L and W are the length and width of the graphene channel, respectively, e is the electronic charge, n_0 is the density of carriers at the maximum resistance (Dirac point), and n is the gate voltage modulated carrier concentration. By fitting this model to the measured data in **Fig. S3**, we can extract the μ and $R_{contact}$. For the 3D GFET without TiO_2 NPs decoration (**Fig. S3a**), μ = 1640 $cm^2\ V^{-1}\ s^{-1}$, and $R_{contact}$ =158 Ω. The mobility of the 3D GFET without TiO_2 NPs decoration is comparable with that of reported 3D GFETs [3]. After coating TiO_2 NPs on the 3D GFETs, the extracted carrier mobility decreases to μ = 1572 $cm^2\ V^{-1}\ s^{-1}$, and the contact resistance increases to $R_{contact}$ = 260 Ω, as shown in **Fig. S3b**. These changes can be attributed to increased disorder caused by

perturbations to the graphene surface during the coating process [4,5].

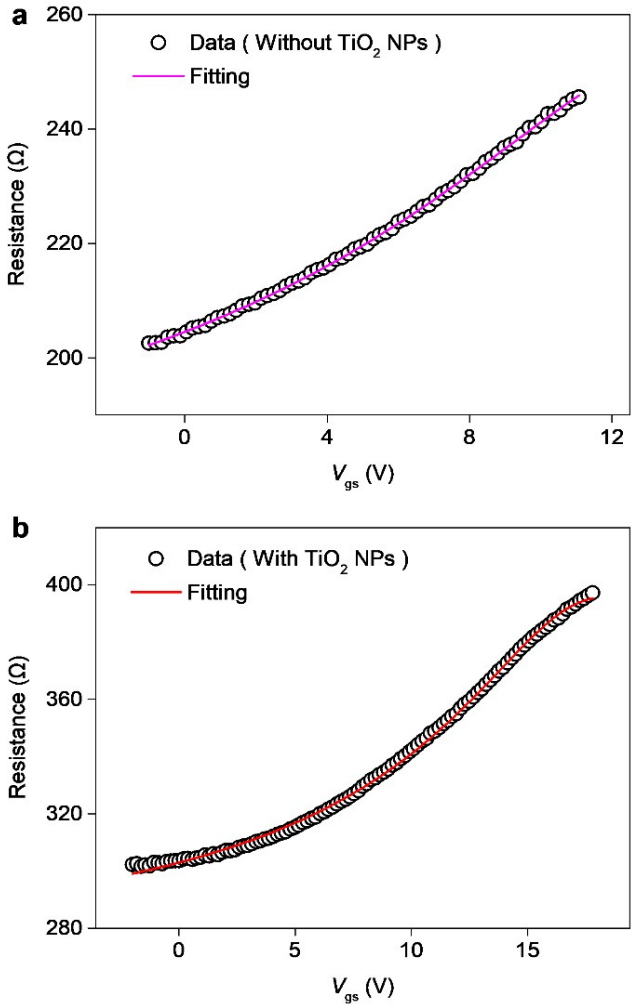

Figure S3 The resistances of the 3D GFET before and after the TiO_2 NPs decoration process. The resistance versus the gate voltage (V_g) along with fitting results for 3D GFETs without (a) and with (b) TiO_2 NPs decoration.

4. Simulation of the optical fields of the 3D GFET and 2D GFET with TiO_2 NPs decoration

The distribution of the electric field magnitude near the 3D GFET and 2D GFET with TiO_2 NPs decorations under 325-nm incident light illumination were simulated using the commercial FEM software Comsol Multiphysics. The 3D rolled-up microcavity was designed in the simulation to ensure that it matched the actual fabricated device as closely as possible.

The microcavity consisted of a 0.335-nm-thick graphene layer, a 30-nm-thick SiO_2 dielectric layer, a 200-nm-thick SiN_x strained layer and a layer of TiO_2 NPs with a diameter of 100 nm. Under the illumination of 325-nm light (laser), the graphene membrane was described using the complex refractive index $n(\lambda) = 3.0 + i(C_1/3)\lambda$, where $C_1 = 5.446\ \mu m^{-1}$ and λ is the wavelength. The SiN_x and SiO_2 layers were modelled as lossless dielectric materials, with refractive indices as shown in **Table S1**.

Table S1 Detailed device structure for simulation

Material	Thickness / diameter (nm)	Refractive index	Bandgap (eV)	Comment
SiN_x	200	1.87	5.1	Strained layers
SiO_2	30	1.45	8.9	Dielectric layer
TiO_2 NPs	100	2.76	3.2	Light harvesters
Graphene	0.335	$3+i\frac{C_1}{3}\lambda$	0	Conductive channel

$C_1 = 5.446\ \mu m^{-1}$, λ is the wavelength.

Reference

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